Pulse Control LSI
PCL6115 / 6125 / 6145
User's Manual

Impress, not just satisfy
Nippon Pulse Motor Co., Ltd.

[Preface]

Thank you for considering our pulse control LSI, the "PCL6100 series."

Before using the product, please read this manual to become familiar with it.

Please note that the section "Handling Precautions", which includes the details of installing these ICs, is shown at the end of this manual.

[Cautions]

(1) Copying all or any part of this manual without written approval is prohibited by copyright laws.

(2) The specifications of these LSIs may be changed to improve performance or quality without prior notice.

(3) Although this manual was produced with the utmost care, if you find any points that are unclear, wrong, or have inadequate descriptions, please let us know.

(4) We are not responsible for any results that may occur from using these LSIs, regardless of item (3) above.

- Explanation of the description in this manual

1. The suffix “x”, “y”, “z”, and “u” of terminal names and bit names refer to X-axis, Y-axis, Z-axis, and U-axis, respectively. The suffix “n” means all axes.
2. Over-lines above negative logic terminal names (ex. RST) are not used in this manual. For the logic, see “3.3 Terminal list”.
3. When describing the bits in registers, “n” refers to a bit position. “0” refers to a bit position and it is prohibited to be written to any other than “0”. This bit always returns “0” when it is read.
4. The specific bit in a status or in a register is shown as follows:
   “Status name. Bit name” or “Register name. Bit name” (e.g. RMD.MSDE)
5. If there is a description of time in this manual, it shows the value at "reference clock frequency of 19.6608 MHz" unless otherwise noted.
6. For “ON” or “OFF” of the signal status, signal status “ON” is shown by “H level” or “1” for the positive logic while “L level” or “0” for the negative logic.
7. As for the suffix attached to numbers, “b” indicates a binary number and “h” indicates a hexadecimal number.
   Suffixes are not attached to decimal numbers.
   Some binary numbers or hexadecimal numbers may not be suffixed when the values are the same in some charts or the decimal numbers.

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1. Outline and features

1.1 Outline

The PCL6115, PCL6125, and PCL6145 are CMOS based Pulse Control LSIs.
They are designed to output high-speed pulses in order to drive stepper motors and servo motors by various commands from CPU.

They provide various types of controls including constant speed, linear acceleration/deceleration, S-curve acceleration/deceleration, command control continuous movement, positioning control incremental movement, and origin return control operation mode, etc.

The number of control axes is; one for the PCL6115, two for the PCL6125, and four for the PCL6145.

The operation status of LSI can be monitored from the CPU, and the LSI can output interrupt signals per a variety of conditions.

They also incorporate functions for servo motor driver control, such as input terminal for In-position signal and output terminal for deviation counter clear signal.

These functions can be controlled with simple commands. Moreover, the intelligent design with the LSI will reduce the burden over the CPU regarding motor controls.

1.2 Features

♦ **3.3 V single voltage power supply**

These LSIs operate by a single 3.3 V power supply.
The output signal level range is 0 V to 3.3 V. The input signal level range is 0 V to 3.3 V or 0 V to 5 V.

♦ **Super high-speed pulse train output**

Up to 9.8 Mpps of command pulses can be output with 19.6608 MHz (standard) reference clock frequency, up to 15 Mpps output is available with 30 MHz (maximum) reference clock.

♦ **CPU bus interface**

These LSIs have built-in parallel bus interface (8-bit: 1 type, 16-bit: 3 types) and a serial bus interface (4-wire synchronous type: 1 type), so that they can be connected to a wide variety of CPUs.

♦ **Acceleration/Deceleration control**

Linear acceleration/deceleration or S-curve acceleration/deceleration is selectable.

Linear acceleration/deceleration sections can be inserted in the middle of an S-curve acceleration/deceleration curve by S-curve section settings.

The S-curve sections can be set differently between acceleration and deceleration.

If the S-curve section is extremely short, such as setting the S-curve section to 1 pps or less, it will appear to be linear acceleration/deceleration. Therefore, you can perform S-curve deceleration after linear acceleration or linear-deceleration after S-curve acceleration.

♦ **Linear interpolation**

These LSIs can perform linear interpolations (= synchronized operations) for any number of axes.

♦ **Target speed override**

Target speed (= operation speed) can be changed during an operation of positioning control incremental movement operation mode. Target speed (= operation speed) and the speed pattern can be changed during an operation of command control continuous movement operation mode.

♦ **Target position override 1) and 2)**

1. Target position (= feeding amount) can be changed during an operation of positioning control incremental movement mode. If the motor position has already exceeded the new target position, it will decelerate and stop (immediate stop in case of constant speed start mode), and then move in the reverse direction.
2. Operation starts in the same way as the continuous movement operation mode until the pulse count start signal is input. If the pulse count start signal is input, LSI will start a positioning control, and can stop when the specified number of pulses is output.

♦ **Triangle drive avoidance (Automatic FH correction)**

In a positioning control incremental movement operation mode, deceleration may start during acceleration if the operation speed (FH speed) is too high for the feeding amount. It is called a triangular drive and it may cause vibration or out-of-step issue. To avoid the issues, operation speed can automatically be reduced so that a triangular drive can be avoided.

♦ **Pre-register**

PCL61x5 LSI has a built-in pre-register (one stage) for storing operation data.

During operation, data for the next operation is set from CPU, and the data can be executed continuously right after the current operation completes.

♦ **Counter circuits**

The following two counters are available separately for each axis.

Counter	Purpose of use	Count Input
COUNTER 1 (RCUN1)	32-bit counter for command position control	Command pulse or encoder signal (EAn/ EBn).
COUNTER 2 (RCUN2)	32-bit counter for mechanical position control	Encoder signal (EAn/EBn) or command pulse

Both counters can be cleared by writing a command. Also, the counter data can be latched by writing a command, a count latch signal, an origin signal, etc. The counters can also be cleared immediately after latching.

♦ **Comparators**

There are 4 comparator circuits for each axis. They can be used to compare target values and internal counter values. Comparator 1 can be compared with COUNTER 1 and Comparator 2 can be compared with COUNTER 2. Comparator 3 and 4 are for software limit function only.

♦ **Simultaneous start**

Multiple axes controlled by one LSI or by multiple LSIs can be started simultaneously by a command or a simultaneous start signal.

♦ **Simultaneous stop**

Multiple axes controlled by one LSI or by multiple LSIs can be stopped simultaneously by a command or a simultaneous stop signal.

♦ **Manual pulser**

By inputting signals with a manual pulser, a motor can be driven directly.

Input signals are 90-degree phase difference signal (1, 2, or 4 multiplication) or 2-pulse signal (up and down pulse signals). It can be stopped within the range of end limit signals or software limit signals on the positive side or the negative side. After being stopped by the end limit signal or software limit range, you can operate only in the opposite direction by reversing the manual pulser signal. You can conduct continuous movement by inputting manual pulser signals or incremental movement to stop at the target position.

♦ **External operation switch**

A motor can be directly driven by inputting an external operation switch signal. The input terminal is shared with manual pulser terminal. The switch signal turns a motor either forward (+ direction) or backward (– direction) and conducts a continuous movement that a motor moves continuously only while the external switch signal is ON or it can conduct an incremental movement that a motor stops at a target position.

♦ **Operation mode**

The basic operations are continuous movement, incremental movement, origin returns, and linear interpolations.

By setting bits for optional operation modes, a variety of operations are available.

<Examples of operation modes>

1) Continuous movement by a command control
2) Continuous movement and incremental movement by pulser control
3) Continuous movement and incremental movement by switch control
4) Origin position return by origin return control
5) Incremental movement by positioning control
6) Hardware start of incremental movement by inputting simultaneous start signal.
7) Incremental movement from the input point of pulse count start signal (target position override 2)

♦ **Origin return sequences**

A variety of origin return controls can be selected by setting of the start command and the optional operation mode bit.

<Examples of origin return sequences>

1) An operation starts at constant speed, and stops immediately when ORG signal turns ON
2) An operation starts at constant speed and stops immediately when a specified number of encoder Z-phase signals is counted after ORG signal turns ON.
3) An operation starts at high-speed and it decelerates when slow-down signal turns ON. It stops immediately when ORG signal turns ON.
4) An operation starts at high-speed, decelerates and stops when ORG signal turns ON.
5) An operation starts at high speed and starts decelerating when ORG signal turns ON. It stops when a specified number of encoder Z-phase signals is counted.

♦ **Mechanical input control**

There are four signal input terminals for each axis as follows:

1. PELn Input a positive direction end limit signal.
   When it turns ON while moving in positive direction, an operation will stop immediately, or decelerate and stop.
   An operation will not start in positive direction if this signal is ON when starts operating. (The negative direction is OK.)
2. MELn Input a negative direction end limit signal.
   When it turns ON while moving in negative direction, an operation will stop immediately, or decelerate and stop.
   An operation will not start in negative direction if this sigal is ON when starts operating. (The positive direction is OK.)
3. SDn Input a slow-down signal.
   When it turns ON while moving, an operation will decelerate or will decelerate and stop.
   If decelerate is set, an operation will decelerate to FL speed when it is ON during high speed start.
   It will operate at FL contstant speed if this signal is ON at start.
   If decelerate & stop is set, an operation will decelerate to FL speed and stop if this sigal is ON during high speed start.
4. ORGn Input an origin signal.
   When it turns ON during an origin return control, an operation will stop immediately, decelerate & stop, or start decelerating.

The input logic of PELn terminal and MELn terminal can be changed by hardware setting.

The input logic of SDn terminal and ORGn terminal can be changed by software settting.

♦ **Servo motor interface**

There are three signal terminals for each axis as follows:

1. INPn Input an in-position signal that is output by a servo motor driver.
2. ERCn Output a deviation counter clear signal that is input to a servo motor driver.
3. ALMn Input an alarm singal that is output by a servo motor driver.
   When this alarm signal is ON, an operation will stop immediately or will decelerate & stop.
   An error interrupt is generated when the alarm signal turns ON even while an operation stops.
   If an alarm signal is ON at start, an operation will never start.

The input logic of INPn and ALMn terminals or the output logic of ERCn terminal can be changed by software setting.

If the pulse output is selected for deviation counter clear signal, the pulse width can be selected;

(From 12 µs to 104 ms, a level output is also available.)

♦ **Output pulse mode**

You can select from common pulse mode, 2-pulse mode and 90-degree phase difference mode. The logic can also be selected.

♦ **Emergency stop signal (CEMG)**

When this signal turns ON, all axes will stop immediately.

If this signal is ON at start, the axis will not start.

♦ **Interrupt request**

An INT signal (interrupt request) can be output from the INT terminal for various factors and reasons.

Interrupt factors for each axis are output from the INT terminal by a logical OR connection.

♦ **General-purpose I/O port**

Each axis has 8-bit general-purpose I/O port.

The I/O specification and logic can be changed by software settings.

♦ **Shared I/O port**

The data bus of parallel bus interface can be used as a 16-bit shared I/O port when a serial bus interface is used.

2. Specification

Item	Description
Number of control axes	PCL6115: One PCL6125: Two (X and Y axes) PCL6145: Four (X, Y, Z, and U axes)
Reference clock frequency (f_{CLK})	Standard: 19.6608 MHz (Max. 30 MHz)
Positioning control range	–2,147,483,648 to +2,147,483,647 (32-bit)
Slow-down point setting range	0 to 16,777,215 (24-bit)
Number of registers used for setting speeds	Two for each axis (FL and FH)
Speed setting step range	1 to 16,383 (14-bit)
Speed magnification range	By changing the reference clock frequency, the speed range will also change with that ratio. 1. When the reference clock frequency = 19.6608 MHz, 0.293× to 600×. (The following is an example.) When 0.3× is selected: 0.3 to 4,914.9 pps When 1× is selected: 1 to 16,383 pps When 600× is selected: 600 to 9,829,800 pps 2. When the reference clock frequency = 30 MHz, 0.447× to 915.527× (The following is an example.) When 0.5× is selected: 0.5 to 8,191.7 pps When 1× is selected: 1 to 16,383.5 pps When 915.527× is selected: 915.527 to 14,999,084.5 pps
Acceleration/Deceleration characteristics	Linear and S-curve acceleration/deceleration. Acceleration and Deceleration characteristics can be set individually.
Acceleration rate setting range	1 to 65,535 (16-bit)
Deceleration rate setting range	1 to 65,535 (16-bit)
Slow-down point automatic setting	The automatic setting is available only when acceleration and deceleration curves are symmetrical.
Triangular drive avoidance (Automatic FH correction)	It will automatically lower the target speed and avoid a triangular drive. A triangular drive is a positioning control that an operation decelerates in the middle of acceleration. It occurs when the feeding amount is too small.
Manual operation input	2 signals; Manual pulser signal (PAn/PBn) and External switch signal (PDR/MDR)
Counters	COUNTER 1 (RCUN1): Command position control counter (32-bit) COUNTER 2 (RCUN2): Mechanical position control counter (32-bit)
Comparators	General-purpose comparators: 32-bit × 2 circuits / axis Software limit only: 32-bit × 2 circuits / axis
CPU bus interface	8-bit parallel bus interface 16-bit parallel bus interface Serial bus interface ($f_{SCK} \leqq \frac{f_{CLK}}{1.5}$)
Interpolation functions	Linear interpolation: Any 2 to 4 axes
Operating temperature range	−40 to +85 °C
Power supply	3.0 to 3.6 V
Package	PCL6115: 80-pin QFP (External dimensions 14 × 14 mm, Mold part 12 × 12 mm) PCL6125: 128-pin QFP (External dimensions 16 × 16 mm, Mold part 14 × 14 mm) PCL6145: 176-pin QFP (External dimensions 26 × 26 mm), Mold part 24 × 24 mm)

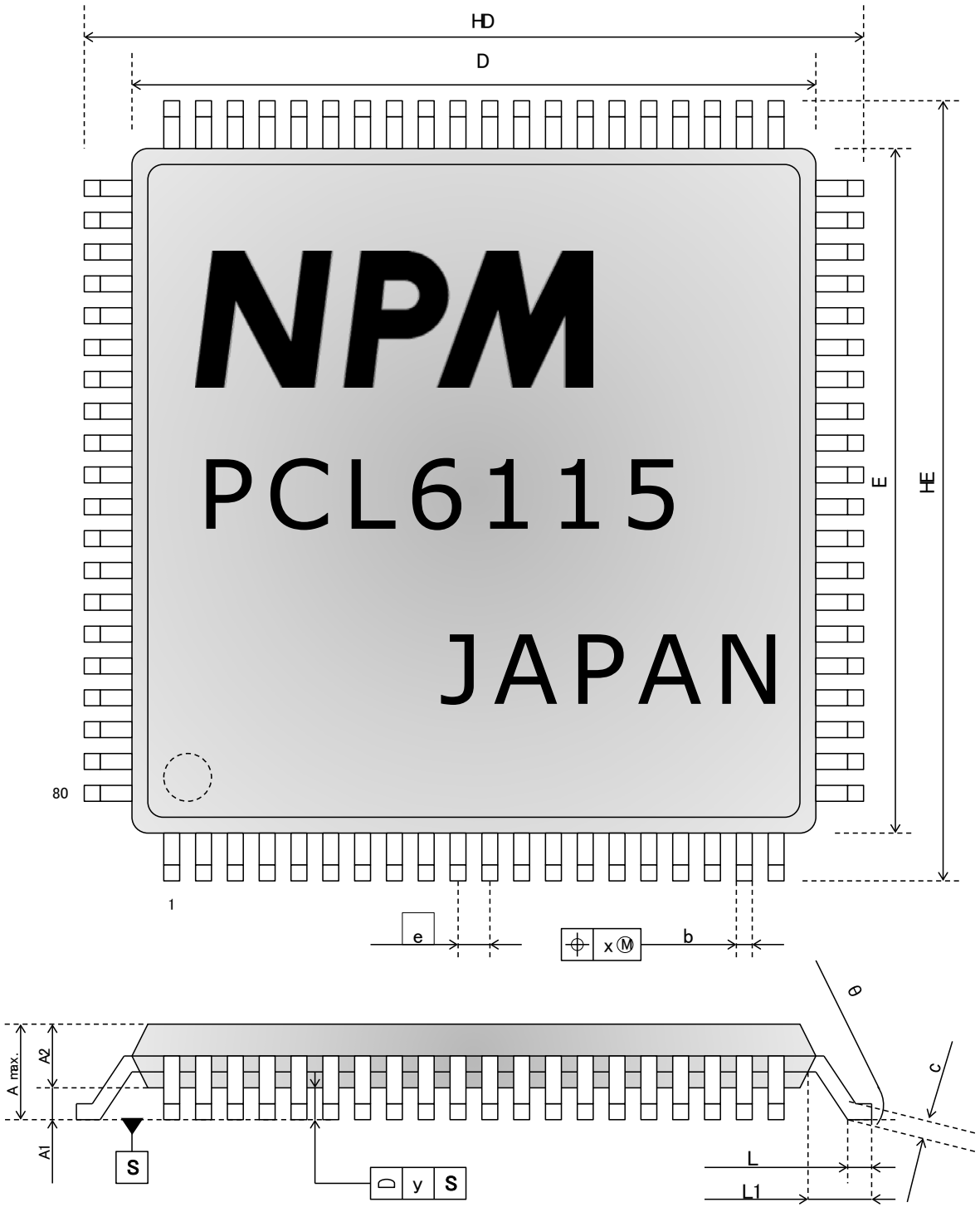
3. Hardware description

The following parts explains the hardware such as external dimensions and terminal layouts.

3.1 External dimensions

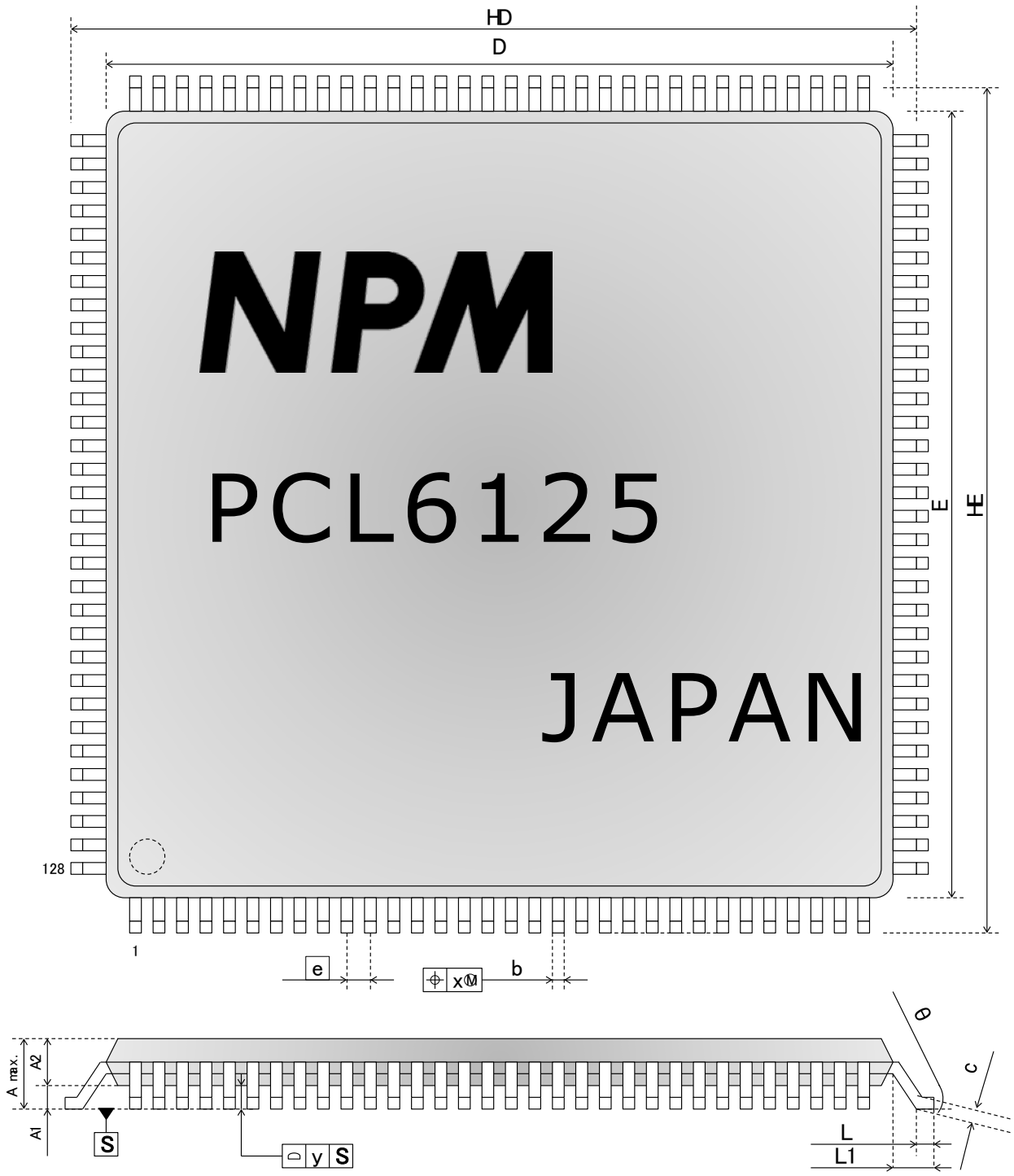
We will explain the external dimensions of each model:

1. PCL6115



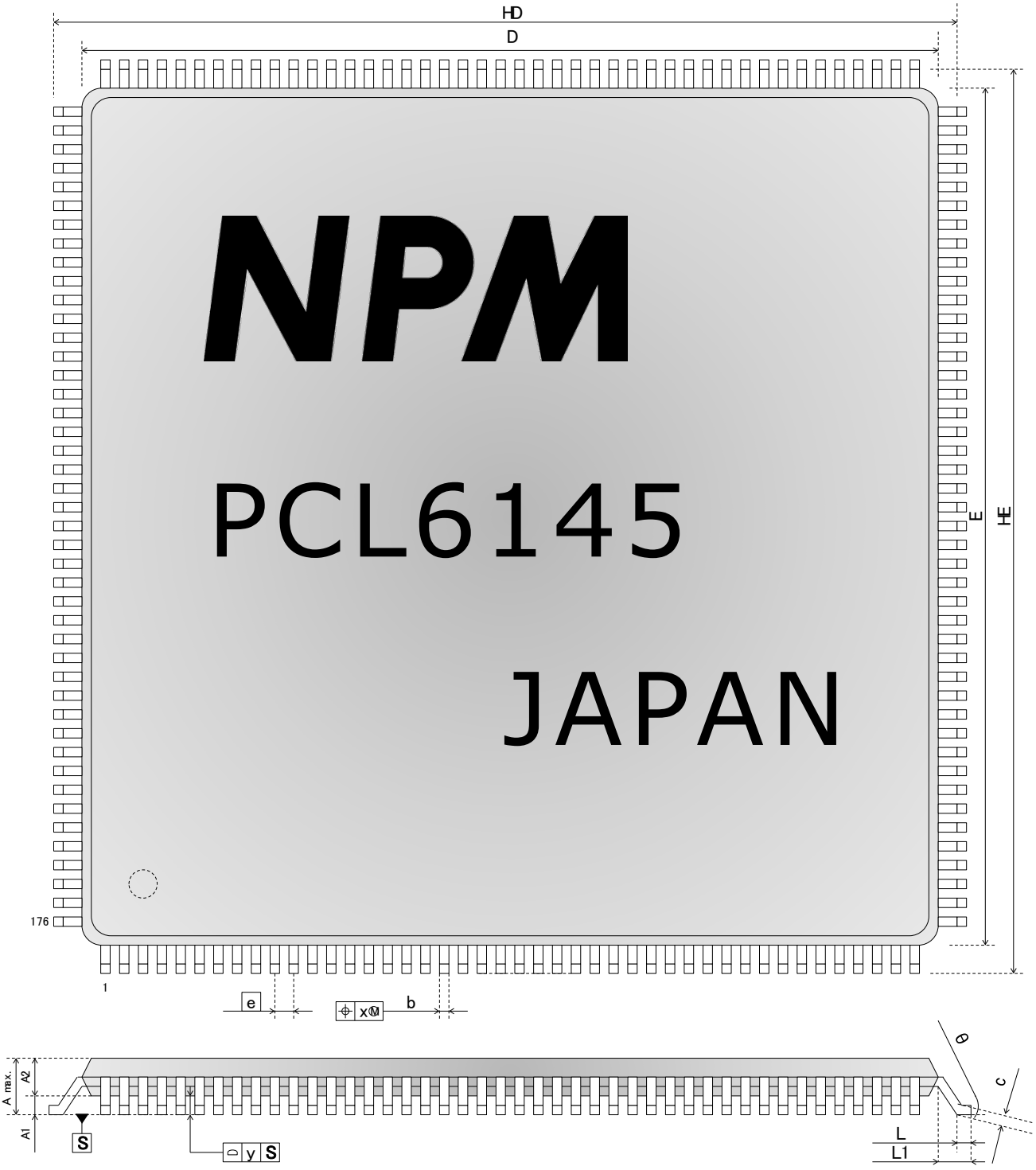
Name	Dimension in mm		
	Min.	Nom.	Max.
E	11.90	12.00	12.10
D	11.90	12.00	12.10
HE	13.60	14.00	14.40
HD	13.60	14.00	14.40
e	-	0.50	-
b	0.13	0.20	0.27
x	-	-	0.08
A max	-	-	1.7
A1	0.00	0.10	0.20
A2	1.30	1.40	1.50
L	0.30	0.50	0.75
L1	0.80	1.00	1.20
θ	0°	5°	10°
c	0.09	0.15	0.20
y	-	-	0.08

2. PCL6125



Name	Dimension in mm		
	Min.	Nom.	Max.
E	13.90	14.00	14.10
D	13.90	14.00	14.10
HE	15.60	16.00	16.40
HD	15.60	16.00	16.40
e	-	0.40	-
b	0.13	0.18	0.23
x	-	-	0.08
A max	-	-	1.70
A1	0.00	0.10	0.20
A2	1.30	1.40	1.50
L	0.30	0.50	0.75
L1	0.80	1.00	1.20
θ	0°	5°	10°
c	0.09	0.15	0.20
y	-	-	0.08

3. PCL6145

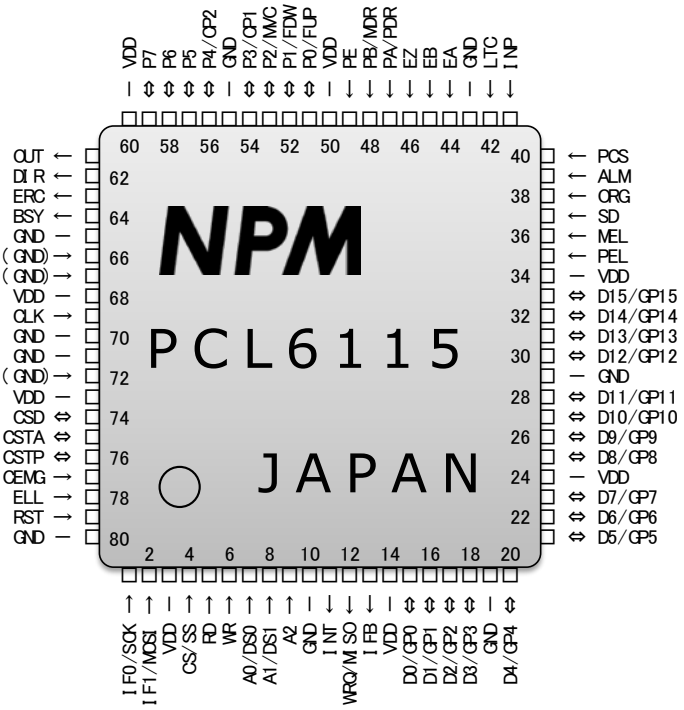


Name	Dimension in mm		
	Min.	Nom.	Max.
E	23.90	24.00	24.10
D	23.90	24.00	24.10
HE	25.60	26.00	26.40
HD	25.60	26.00	26.40
e	-	0.50	-
b	0.17	0.22	0.27
x	-	-	0.08
A max	-	-	1.70
A1	0.00	0.10	0.20
A2	1.30	1.40	1.50
L	0.30	0.50	0.75
L1	0.80	1.00	1.20
θ	0°	5°	10°
c	0.09	0.15	0.20
y	-	-	0.08

3.2 Terminal assignment diagrams

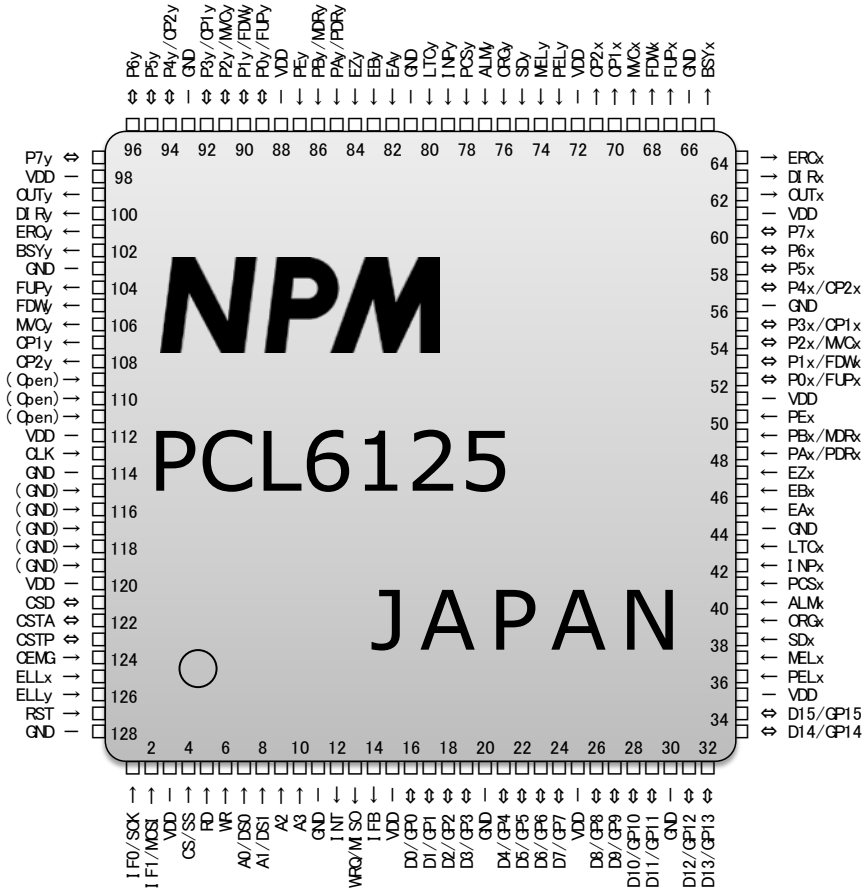
The following shows the terminal assignments of each LSI.

1. PCL6115



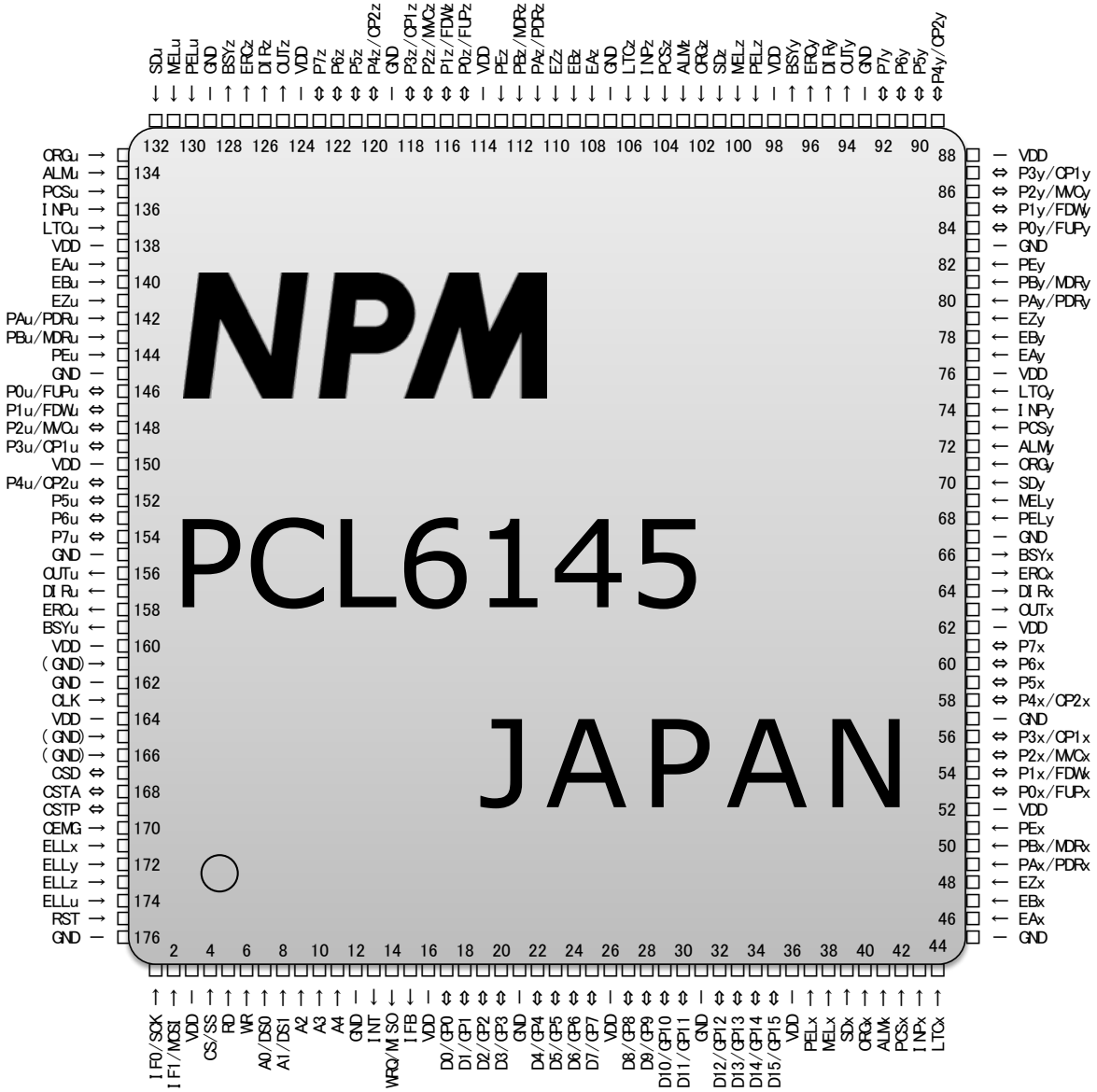
Note: The terminal pin at the lower left side is # 1.

2. PCL6125



Note: The terminal pin at the lower left side is # 1.

3. PCL6145



Note: The terminal pin at the lower left corner is # 1.

3.3 Terminal list

Note:

1. [Direction] column indicates the signal direction; “I” means input, “O” means output, and “B” means bi-directional.
2. [Logic] column indicates the signal logic; “P” means positive logic, “N” means negative logic. “#” means changeable with software. “%” means set by hardware
3. [Handling] column describes how to deal with the terminals when they are not used.
   Some terminals need to be processed when they are used.
   “OP” means to leave open, “PU” means to pull up, “PU (PD)” means to pull-up or to pull-down, “+V” means to connect directly to VDD or to pull up, and “GN” means to connect directly to GND or to pull- down. A resistance value of 5k to 10k ohm is recommended.
4. 0 V to +5 V level can be input to input terminals of all signals.
5. The output terminals of all signals can be pulled up to +5 V. However, equal to or more than VDD cannot be output. (Equal to or more than 5k ohm resistant value is recommended.)

3.3.1 PCL6115

Terminal No.	Signal name	Direction	Logic	Handling	Description
1	IF0/SCK	I	-	-	Parallel bus interface: Sets CPU bus interface mode. Serial bus interface: Inputs the serial clock signal.
2	IF1/MOSI	I	-	-	Parallel bus interface: Sets CPU bus interface mode. Serial bus interface: Inputs I/O data from CPU.
3	VDD	-	-	-	Power supply terminal. Connect to 3.3 V.
4	CS/SS	I	N	-	Parallel bus interface: Inputs a chip select signal. Serial bus interface: Inputs the slave select signal.
5	RD	I	N	-	Parallel bus interface: Inputs a read signal. Serial bus interface: Connects to GND.
6	WR	I	N		Parallel bus interface: Inputs a write signal. Serial bus interface: Connects to GND.
7 8	A0 / DS0 A1 / DS1	I	P	-	Parallel bus interface: Inputs an address signal. Serial bus interface: Sets the device select number.
9	A2	I	P	PU (PD)	Parallel bus interface: Inputs an address signal. Serial bus interface: Sets the device select number.
10	GND	-	-	-	Power supply terminal. Connects to GND.
11	INT	O	N	OP	Outputs an interrupt request signal. See “7.13 Interrupt (INT) function” for details.

Terminal No.	Signal name	Direction	Logic	Handling	Description
12	WRQ/MISO	O	N	OP	Parallel bus interface: Outputs a wait request signal. Serial bus interface: Outputs the input data to CPU.
13	IFB	O	N	OP	Parallel bus interface: Outputs an interface busy signal. Serial bus interface: Leave it Open.
14	VDD				Power supply terminal. Connects to 3.3 V.
15 16 17 18	D0/GP0 D1/GP1 D2/GP2 D3/GP3	B	P	PU (PD)	Parallel bus interface: Connect data bus; Bit 0 to Bit 3. Serial bus interface: Become shared I/O ports; GP0 to GP3 terminals.
19	GND	-	-	-	Power supply terminal. Connects to GND.
20 21 22 23	D4/GP4 D5/GP5 D6/GP6 D7/GP7	B	P	PU (PD)	Parallel bus interface: Connect data bus; Bit 4 to Bit 7. Serial bus interface: Become shared I/O ports; GP4 to GP7 terminals.
24	VDD	-	-	-	Power supply terminal. Connects to 3.3 V.
25 26 27 28	D8/GP8 D9/GP9 D10/GP10 D11/GP11	B	P	PU (PD)	Parallel bus interface: Connect 16-bit data bus; Bit 8 to Bit 11. 8-bit data bus needs to be pulled-up or pulled-down. Serial bus interface: Become shared I/O ports; GP8 to GP11 terminals.
29	GND	-	-	-	Power supply terminal. Connects to GND.
30 31 32 33	D12/GP12 D13/GP13 D14/GP14 D15/GP15	B	P	PU (PD)	Parallel bus interface: Connect 16-bit data bus; Bit 12 to Bit 15. 8-bit data bus needs to be pulled up or pulled down. Serial bus interface: Become shared I/O ports; GP12 to GP15 terminals.
34	VDD	-	-	-	Power supply terminal. Connects to 3.3 V.
35	PEL	I	N%	+V	Inputs an end limit signal on the positive side. See “7.4.1 End limit signal (PELn, MELn) for details”.
36	MEL	I	N%	+V	Inputs an end limit signal on the negative side. See “7.4.1 End limit signal (PELn, MELn) for details”.

Terminal No.	Signal name	Direction	Logic	Handling	Description
37	SD	I	N#	+V	Inputs a slow-down signal. See “7.4.2 Slow-down signal (SDn)” for details.
38	ORG	I	N#	+V	Inputs an origin position signal. See “7.4.3 Origin position signal (ORGn), encoder Z-phase signal (EZn)” for details.
39	ALM	I	N#	+V	Inputs an alarm signal input from a servo motor driver. See “7.5.3 Alarm signals (ALMn)” for details.
40	PCS	I	N#	GN	Inputs a pulse count start signal or an own-axis start signal. See "7.2.2 Target position override 2 (PCSn)" or "7.6.2 Own-axis start signal (PCSn)" for details.
41	INP	I	N#	GN	Inputs an in-position signal from a servo motor driver. See "7.5.1 In-position signal (INPn)” for details.
42	LTC	I	N#	GN	Inputs a counter latch signal. See “7.10.2 Latch and clear (LTCn)” for details.
43	GND	-	-	-	Power supply terminal. Connects to GND.
44	EA	I	-	GN	Inputs A-phase signals from an encoder. See “7.10.1 Counter type and input specification” for details.
45	EB	I	-	GN	Inputs B-phase signals from an encoder. See “7.10.1 Counter type and input specification” for details.
46	EZ	I	N#	GN	Inputs Z-phase signals from an encoder. See “7.4.3 Origin position signal (ORGn), encoder Z-phase signal (EZn)” for details.
47	PA/PDR	I	-	GN	Connects to A-phase of a manual pulser or on the positive side of an external switch. See “5.3 Manual pulser control” or “5.4 Switch control” for details.
48	PB/MDR	I	-	GN	Connects to B-phase of a manual pulser or on the negative side of an external switch. See “5.3 Manual pulser control” or “5.4 Switch control” for details.
49	PE	I	N	GN	Inputs enable signals of a manual pulser as well as an external switch. L level (GN): Controllable by PA/PDR terminals and PB/MDR terminals. H level (+V): Uncontrollable by PA/PDR terminals and PB/MDR terminals.
50	VDD	-	-	-	Power supply terminal. Connects to 3.3 V.

Terminal No.	Signal name	Direction	Logic	Handling	Description
51	P0/FUP	B	-	PU (PD)	P0 terminal used for a general-purpose I/O port or an output terminal for on-going acceleration signals. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
52	P1/FDW	B	-	PU (PD)	P1 terminal used for a general-purpose I/O port or an output terminal for on-going slow-down signals. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
53	P2/MVC	B	-	PU (PD)	P2 terminal used for a general-purpose I/O port or an output terminal for on-going constant speed operation signals. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
54	P3/CP1	B	-	PU (PD)	P3 terminal used for a general-purpose I/O port or an output a signal indicating comparator 1 condition is met. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
55	GND	-	-	-	Power supply terminal. Connects to GND.
56	P4/CP2	B	-	PU (PD)	P4 terminal used for a general purpose I/O port or an output a signal indicating comparator 2 condition is met. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
57	P5	B	-	PU (PD)	P5 terminal used for a general purpose I/O port. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
58	P6	B	-	PU (PD)	P6 terminal used for a general purpose I/O port. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
59	P7	B	-	PU (PD)	P7 terminal used for a general purpose I/O port See “4.4.4.3 RENV2: Environment setting 2 register” for details.
60	VDD	-	-	-	Power supply terminal. Connects to 3.3 V.
61	OUT	O	N#	OP	Outputs a command pulse to a motor driver. See “7.3.1 Output pulse mode (OUTn, DIRn)” for details.
62	DIR	O	N#	OP	Outputs a command pulse to a motor driver. See “7.3.1 Output pulse mode (OUTn, DIRn)” for details.
63	ERC	O	N#	OP	Outputs a deviation counter clear signal to a servo motor driver. See “7.5.2 Deviation counter clear signal (ERCn)” for details.
64	BSY	O	N	OP	Outputs a signal to indicate that an operation is busy. It becomes L level during operation.
65	GND	-	-	-	Power supply terminal. Connects to GND.
66 67	(GND)	I	-	GN	Input terminal for shipping inspection. Connects to GND.
68	VDD	-	-	-	Power supply terminal. Connects to 3.3 V.

Terminal No.	Signal name	Direction	Logic	Handling	Description
69	CLK	I	-	-	Inputs the reference clock (CLK) signal. Standard frequency is 19.6608 MHz.
70	GND	-	-	-	Power supply terminal Connects to GND.
71	GND	-	-	-	Power supply terminal Connects to GND.
72	(GND)	I	-	GN	Input terminal for shipping inspection. Connects to GND.
73	VDD	-	-	-	Power supply terminal Connects to 3.3 V.
74	CSD	B	N	PU	Inputs/Outputs a simultaneous slow-down signal. See “7.7.1 Simultaneous slow-down signal (CSD)” for details.
75	CSTA	B	N	PU	Inputs/Outputs a simultaneous start signal. See “7.6.1 Simultaneous start signal (CSTA)” for details.
76	CSTP	B	N	PU	Inputs/Outputs a simultaneous stop signal. See “7.8.1 Simultaneous stop signal (CSTP)” for details.
77	CEMG	I	N	+V	Inputs an emergency stop signal. See “7.9.1 Emergency stop signal (CEMG)” for details.
78	ELL	I	-	-	Selects the input logic of an end limit signal. L level (GN): Input logic is positive. H level (+V): Input logic is negative.
79	RST	I	N	-	Inputs a reset signal. See “7.1 Reset” for details.
80	GND	-	-	-	Power supply terminal Connects to GND.

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Terminal No.	Signal name	Direction	Logic	Handling	Description
1	IF0/SCK	I	-	-	Parallel bus interface: Sets CPU bus interface mode. Serial bus interface: Inputs a serial clock signal.
2	IF1/MOSI	I	-	-	Parallel bus interface: Sets CPU bus interface mode. Serial bus interface: Inputs I/O data from CPU.
3	VDD	-	-	-	Power supply terminal Connects to 3.3 V.
4	CS/SS	I	N	-	Parallel bus interface: Inputs a chip select signal. Serial bus interface: Inputs a slave select signal.
5	RD	I	N	-	Parallel bus interface: Inputs a read signal. Serial bus interface: Connects to GND.
6	WR	I	N	-	Parallel bus interface: Inputs a write signal. Serial bus interface: Connects to GND.
7 8	A0 / DS0 A1 / DS1	I	P	-	Parallel bus interface: Inputs an address signal. Serial bus interface: Sets a device select number.
9 10	A2 A3	I	P	PU (PD)	Parallel bus interface: Inputs an address signal. Serial bus interface: To be pulled up or pulled down.
11	GND	-	-	-	Power supply terminal. Connects to GND.
12	INT	O	N	OP	Outputs an interrupt request signal. See “7.13 Interrupt (INT) function” for details.
13	WRQ/MISO	O	N	OP	Parallel bus interface: Outputs a wait request signal. Serial bus interface: Outputs an input data to CPU.
14	IFB	O	N	OP	Parallel bus interface: Outputs an interface busy signal. Serial bus interface: Leave it Open.
15	VDD	-	-	-	Power supply terminal. Connects to 3.3 V.
16 17 18 19	D0/GP0 D1/GP1 D2/GP2 D3/GP3	B	P	PU (PD)	Parallel bus interface: Connect data bus; Bit 0 to Bit 3. Serial bus interface: Become shared I/O ports; GP0 to GP3 terminals.
20	GND	-	-	-	Power supply terminal Connects to GND.

Terminal No.	Signal name	Direction	Logic	Handling	Description
21 22 23 24	D4/GP4 D5/GP5 D6/GP6 D7/GP7	B	P	PU (PD)	Parallel bus interface: Connect data bus; Bit 4 to Bit 7. Serial bus interface: Become-shared I/O ports; GP4 to GP7 terminals.
25	VDD	-	-	-	Power supply terminal Connects to 3.3 V.
26 27 28 29	D8/GP8 D9/GP9 D10/GP10 D11/GP11	B	P	PU (PD)	Parallel bus interface: Connect 16-bit data bus; Bit 8 to Bit 11. 8-bit data bus needs to be pulled up or pulled down. Serial bus interface: Become shared I/O ports; GP8 to GP11 terminals.
30	GND	-	-	-	Power supply terminal Connects to GND.
31 32 33 34	D12/GP12 D13/GP13 D14/GP14 D15/GP15	B	P	PU (PD)	Parallel bus interface: Connect 16-bit data bus; Bit 12 to Bit 15. 8-bit data bus needs to be pulled up or pulled down. Serial bus interface: Become shared I/O ports; GP12 to GP15 terminals.
35	VDD	-	-	-	Power supply terminal Connects to 3.3 V.
36	PELx	I	N%	+V	Inputs an end limit signal on the positive side. See “7.4.1 End limit signal (PELn, MELn)” for details.
37	MELx	I	N%	+V	Inputs end limit signal on the negative side. See “7.4.1 End limit signal (PELn, MELn)” for details.
38	SDx	I	N#	+V	Input a slow-down signal. See “7.4.2 Slow-down signal (SDn)” for details.
39	ORGx	I	N#	+V	Inputs an origin position signal. See “7.4.3 Origin position signal (ORGn), encoder Z-phase signal (EZn)” for details.
40	ALMx	I	N#	+V	Inputs an alarm signal input from a servo motor driver. See “7.5.3 Alarm signals (ALMn)” for details.
41	PCSx	I	N#	GN	Inputs a pulse count start signal or an own-axis start signal. See "7.2.2 Target position override 2 (PCSn)" or "7.6.2 Own-axis start signal (PCSn)" for details.
42	INPx	I	N#	GN	Inputs an in-position signal from a servo driver. See "7.5.1 In-position signal (INPn)” for details.

Terminal No.	Signal name	Direction	Logic	Handling	Description
43	LTCx	I	N#	GN	Inputs a counter latch signal. See “7.10.2 Latch and clear (LTCn)” for details.
44	GND	-	-	-	Power supply terminal Connects to GND.
45	EAx	I	-	GN	Inputs A-phase signals from an encoder. See “7.10.1 Counter type and input specification” for details.
46	EBx	I	-	GN	Inputs B-phase signals from an encoder. See “7.10.1 Counter type and input specification” for details.
47	EZx	I	N#	GN	Inputs Z-phase signals from an encoder. See “7.4.3 Origin position signal (ORGn), encoder Z-phase signal (EZn)” for details.
48	PAx/PDRx	I	-	GN	Connects to A-phase of a manual pulser or the positive direction of an external switch. See “5.3 Manual pulser control” or “5.4 Switch control” for details.
49	PBx/MDRx	I	-	GN	Connects to B-phase of a manual pulser or the negative direction of an external switch. See “5.3 Manual pulser control” or “5.4 Switch control” for details.
50	PEx	I	N	GN	Inputs enable signals of manual pulser as well as the external switch. L level (GN): Controllable by PAx/PDRx terminals and PBx/MDRx terminals. H level (+V): Uncontrollable by PAx/PDRx terminals and PBx/MDRx terminals.
51	VDD	-	-	-	Power supply terminal Connects to 3.3 V.
52	P0x/FUPx	B	-	PU (PD)	P0 terminal used for a general purpose I/O port or an output terminal for on-going acceleration signal. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
53	P1x/FDWx	B	-	PU (PD)	P1 terminal used for a general purpose I/O port or an output terminal for on-going slow-down signal. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
54	P2x/MVCx	B	-	PU (PD)	P2 terminal used for a general purpose I/O port or an output terminal for on-going constant speed operation signal. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
55	P3x/CP1x	B	-	PU (PD)	P3 terminal used for a general-purpose I/O port or outputs a signal indicating comparator 1 condition is met. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
56	GND	-	-	-	Power supply terminal Connects to GND.
57	P4x/CP2x	B	-	PU (PD)	P4 terminal used for general purpose I/O port or output a signal indicating comparator 2 condition is met. See “4.4.4.3 RENV2: Environment setting 2 register” for details.

Terminal No.	Signal name	Direction	Logic	Handling	Description
58	P5x	B	-	PU (PD)	P5 terminal used for a general purpose I/O port See “4.4.4.3 RENV2: Environment setting 2 register” for details.
59	P6x	B	-	PU (PD)	P6 terminal used for a general purpose I/O port See “4.4.4.3 RENV2: Environment setting 2 register” for details.
60	P7x	B	-	PU (PD)	P7 terminal used for a general purpose I/O port See “4.4.4.3 RENV2: Environment setting 2 register” for details.
61	VDD	-	-	-	Power supply terminal Connects to 3.3 V.
62	OUTx	O	N#	OP	Outputs a command pulse to a motor driver. See “7.3.1 Output pulse mode (OUTn, DIRn)” for details.
63	DIRx	O	N#	OP	Outputs a command pulse to a motor driver. See “7.3.1 Output pulse mode (OUTn, DIRn)” for details.
64	ERCx	O	N#	OP	Outputs a deviation counter clear signal to a servo motor driver. See “7.5.2 Deviation counter clear signal (ERCn)” for details.
65	BSYx	O	N	OP	Outputs a signal to indicate that an operation is busy. It becomes L level during operation.
66	GND	-	-	-	Power supply terminal Connects to GND.
67	FUPx	O	N	OP	Outputs signals during acceleration. It becomes L level during acceleration.
68	FDWx	O	N	OP	Outputs signals during deceleration. It becomes L level during deceleration.
69	MVCx	O	N	OP	Outputs signals during constant speed operation. It becomes L level during operation.
70	CP1x	O	N	OP	Outputs a signal when the condition of comparator 1 is met. It becomes L level when comparator 1 is met.
71	CP2x	O	N	OP	Outputs a signal when the condition of comparator 2 is met. It becomes L level when comparator 2 is met.
72	VDD	-	-	-	Power supply terminal Connects to 3.3 V.
73	PELy	I	N%	+V	Inputs an end limit signal on the positive side. See “7.4.1 End limit signal (PELn, MELn)” for details.
74	MELy	I	N%	+V	Inputs an end limit signal on the negative side. See “7.4.1 End limit signal (PELn, MELn)” for details.

Terminal No.	Signal name	Direction	Logic	Handling	Description
75	SDy	I	N#	+V	Inputs a slow-down signal. See “7.4.2 Slow-down signal (SDn)” for details.
76	ORGy	I	N#	+V	Inputs an origin position signal. See “7.4.3 Origin position signal (ORGn), encoder Z-phase signal (EZn)” for details.
77	ALMy	I	N#	+V	Inputs an alarm signal input from a servo motor driver. See “7.5.3 Alarm signals (ALMn)” for details.
78	PCSy	I	N#	GN	Inputs a pulse count start signal or an own-axis start signal. See “7.2.2 Target position override 2 (PCSn)” or “7.6.2 Own-axis start signal (PCSn)” for details.
79	INPy	I	N#	GN	Inputs an in-position signal input from a servo motor driver. See "7.5.1 In-position signal (INPn)” for details.
80	LTCy	I	N#	GN	Input counter latch signals. See “7.10.2 Latch and clear (LTCn)” for details.
81	GND	-	-	-	Power supply terminal Connects to GND.
82	EAy	I	-	GN	Inputs A-phase signals from an encoder. See “7.10.1 Counter type and input specification” for details.
83	EBy	I	-	GN	Inputs B-phase signals from an encoder. See “7.10.1 Counter type and input specification” for details.
84	EZy	I	N#	GN	Inputs Z-phase signals from an encoder. See “7.4.3 Origin position signal (ORGn), encoder Z-phase signal (EZn)” for details.
85	PAy/PDRy	I	-	GN	Connects to A-phase of a manual pulser or the positive direction of an external switch. See “5.3 Manual pulser control” or “5.4 Switch control” for details.
86	PBy/MDRy	I	-	GN	Connects to B-phase of a manual pulser or the negative direction of an external switch. See “5.3 Manual pulser control” or “5.4 Switch control” for details.
87	PEy	I	N	GN	Inputs manual pulser signals or external switch enable signals. L level (GN): Controllable by PAy/PDRy and PBy/MDRy terminals. H level (+V): Uncontrollable by PAy/PDRy and PBy/MDRy terminals.
88	VDD	-	-	-	Power supply terminal Connects to 3.3 V.

Terminal No.	Signal name	Direction	Logic	Handling	Description
89	P0y/FUPy	B	-	PU (PD)	P0 terminal used for a general purpose I/O port or an output terminal for on-going acceleration signal. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
90	P1y/FDWy	B	-	PU (PD)	P1 terminal used for a general purpose I/O port or an output terminal for on-going slow-down signal. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
91	P2y/MVCy	B	-	PU (PD)	P2 terminal used for a general purpose I/O port or an output terminal for on-going constant speed operation signal. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
92	P3y/CP1y	B	-	PU (PD)	P3 terminal used for a general purpose I/O port or an output terminal for signal that indicates the condition of comparator 1 is met. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
93	GND	-	-	-	Power supply terminal. Connects to GND.
94	P4y/CP2y	B	-	PU (PD)	P4 terminal used for a general purpose I/O port or an output terminal for signal that indicates the condition of comparator 2 is met. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
95	P5y	B	-	PU (PD)	P5 terminal used for a general purpose I/O port. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
96	P6y	B	-	PU (PD)	P6 terminal used for a general purpose I/O port. See “4.4.4.3 RENV2: Environment setting 2 register” for details
97	P7y	B	-	PU (PD)	P7 terminal used for a general purpose I/O port. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
98	VDD	-	-	-	Power supply terminal. Connects to 3.3 V.
99	OUTy	O	N#	OP	Outputs a command pulse to a motor driver. See “7.3.1 Output pulse mode (OUTn, DIRn)” for details.
100	DIRy	O	N#	OP	Outputs a command pulse to a motor driver. See “7.3.1 Output pulse mode (OUTn, DIRn)” for details.
101	ERCy	O	N#	OP	Outputs a deviation counter clear signal to a servo motor driver. See “7.5.2 Deviation counter clear signal (ERCn)” for details.
102	BSYy	O	N	OP	Outputs signals to indicate that an operation is busy. It becomes to L level during operation.
103	GND	-	-	-	Power supply terminal Connects to GND.
104	FUPy	O	N	OP	Outputs signals during acceleration. It becomes L level during acceleration.
105	FDWy	O	N	OP	Outputs signals during deceleration. It becomes L level during deceleration.

Terminal No.	Signal name	Direction	Logic	Handling	Description
106	MVCy	O	N	OP	Outputs constant speed signals. It becomes L level during constant speed operation.
107	CP1y	O	N	OP	Outputs a signal when the condition of comparator 1 is met. It becomes L level while the condition of comparator 1 is met.
108	CP2y	O	N	OP	Outputs signal when the condition of comparator 2 is met. It becomes L level while the condition of comparator 2 is met.
109 110 111	(Open)	O	-	OP	Input terminal for shipping inspection. Leave it open.
112	VDD	-	-	-	Power supply terminal Connects to 3.3 V.
113	CLK	I	-	-	Inputs reference clock (CLK) signals. Standard frequency is 19.6608 MHz.
114	GND	-	-	-	Power supply terminal Connects to GND.
115 116 117 118 119	(GND)	I	-	GN	Input terminal for shipping inspection. Connects to GND.
120	VDD	-	-	-	Power supply terminal Connects to 3.3 V.
121	CSD	B	N	PU	Inputs or outputs a simultaneous slow-down signal. See “7.7.1 Simultaneous slow-down signal (CSD)” for details.
122	CSTA	B	N	PU	Inputs or outputs a simultaneous start signal. See “7.6.1 Simultaneous start signal (CSTA)” for details.
123	CSTP	B	N	PU	Inputs or outputs a simultaneous stop signal. See “7.8.1 Simultaneous stop signal (CSTP)” for details.
124	CEMG	I	N	+V	Inputs an emergency stop signal. See “7.9.1 Emergency stop signal (CEMG)” for details.
125	ELLx	I	-	-	Selects the input logic for an end limit signal. L level (GN): Input logic is positive. H level (+V): Input logic is negative.

Terminal No.	Signal name	Direction	Logic	Handling	Description
126	ELLy	I	-	-	Selects the input logic for end limit signal. L level (GN): Input logic is positive. H level (+V): Input logic is negative.
127	RST	I	N	-	Inputs a reset signal. See “7.1 Reset” for details.
128	GND	-	-	-	Power supply terminal Connects to GND.

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Terminal No.	Signal name	Direction	Logic	Handling	Description
1	IF0/SCK	I	-	-	Parallel bus interface: Sets CPU bus interface mode. Serial bus interface: Input a serial clock signal.
2	IF1/MOSI	I	-	-	Parallel bus interface: Sets CPU bus interface mode. Serial bus interface: I/O data from CPU.
3	VDD	-	-	-	Power supply terminal Connects to 3.3 V.
4	CS/SS	I	N	-	Parallel bus interface: Inputs a chip select signal. Serial bus interface: Inputs a slave select signal.
5	RD	I	N	-	Parallel bus interface: Inputs a read signal. Serial bus interface: Connects to GND.
6	WR	I	N	-	Parallel bus interface: Inputs a write signal. Serial bus interface: Connects to GND.
7 8	A0/DS0 A1/DS1	I	P	-	Parallel bus interface: Inputs an address signal. Serial bus interface: Sets device select number.
9 10 11	A2 A3 A4	I	P	PU (PD)	Parallel bus interface: Inputs an address signal. Serial bus interface: To be pulled up or pulled down.
12	GND	-	-	-	Power supply terminal. Connects to GND.
13	INT	O	N	OP	Outputs an interrupt request signal. See “7.13 Interrupt (INT) function” for details.
14	WRQ/MISO	O	N	OP	Parallel bus interface: Outputs a wait request signal. Serial bus interface: Outputs an input data to CPU.
15	IFB	O	N	OP	Parallel bus interface: Outputs an interface busy signal. Serial bus interface: Leave it Open.
16	VDD	-	-	-	Power supply terminal. Connects to 3.3 V.
17 18 19 20	D0/GP0 D1/GP1 D2/GP2 D3/GP3	B	P	PU (PD)	Parallel bus interface: Connects data bus; Bit 0 to Bit 3. Serial bus interface: Become shared I/O ports; GP0 to GP3 terminals.
21	GND	-	-	-	Power supply terminal Connects to GND.

Terminal No.	Signal name	Direction	Logic	Handling	Description
22 23 24 25	D4/GP4 D5/GP5 D6/GP6 D7/GP7	B	P	PU (PD)	Parallel bus interface: Connect data bus; Bit 4 to Bit 7. Serial bus interface: Become shared I/O ports; GP4 to GP7 terminals.
26	VDD	-	-	-	Power supply terminal Connects to 3.3 V.
27 28 29 30	D8/GP8 D9/GP9 D10/GP10 D11/GP11	B	P	PU (PD)	Parallel bus interface: Connect 16-bit data bus; Bit 8 to Bit 11. 8-bit data bus needs to be pulled up or pulled down. Serial bus interface: Become shared I/O ports; GP8 to GP11 terminals.
31	GND	-	-	-	Power supply terminal Connects to GND
32 33 34 35	D12/GP12 D13/GP13 D14/GP14 D15/GP15	B	P	PU (PD)	Parallel bus interface: Connect 16-bit data bus; Bit 12 to Bit 15. 8-bit data bus needs to be pulled up or pulled down. Serial bus interface: Become shared I/O ports; GP12 to GP15 terminals.
36	VDD	-	-	-	Power supply terminal Connects to 3.3 V.
37	PELx	I	N%	+V	Inputs an end limit signal on the positive side. See “7.4.1 End limit signal (PELn, MELn)” for details.
38	MELx	I	N%	+V	Inputs an end limit signal on the negative side. See “7.4.1 End limit signal (PELn, MELn)” for details.
39	SDx	I	N#	+V	Input a slow-down signal. See “7.4.2 Slow-down signal (SDn)” for details.
40	ORGx	I	N#	+V	Inputs an origin position signal. See “7.4.3 Origin position signal (ORGn), encoder Z-phase signal (EZn)” for details.
41	ALMx	I	N#	+V	Inputs an alarm signal input from a servo motor driver. See “7.5.3 Alarm signals (ALMn)” for details.
42	PCSx	I	N#	GN	Inputs a pulse count start signal or an own-axis start signal. See “7.2.2 Target position override 2 (PCSn)” or “7.6.2 Own-axis start signal (PCSn)” for details.
43	INPx	I	N#	GN	Inputs an in-position signal from a servo driver. See "7.5.1 In-position signal (INPn)” for details.

Terminal No.	Signal name	Direction	Logic	Handling	Description
44	LTCx	I	N#	GN	Inputs counter latch signals. See “7.10.2 Latch and clear (LTCn)” for details.
45	GND	-	-	-	Power supply terminal. Connects to GND.
46	EAx	I	-	GN	Inputs A-phase signals from an encoder. See “7.10.1 Counter type and input specification” for details.
47	EBx	I	-	GN	Inputs B-phase signals from an encoder. See “7.10.1 Counter type and input specification” for details.
48	EZx	I	N#	GN	Inputs Z-phase signals from an encoder. See “7.4.3 Origin position signal (ORGn), encoder Z-phase signal (EZn)” for details.
49	PAx/PDRx	I	-	GN	Connects to A-phase of a manual pulser or the positive direction of an external switch. See “5.3 Manual pulser control” or “5.4 Switch control” for details.
50	PBx/MDRx	I	-	GN	Connects to B-phase of a manual pulser or the negative direction of an external switch. See “5.3 Manual pulser control” or “5.4 Switch control” for details.
51	PEx	I	N	GN	Inputs enable signals of a manual pulser as well as external switch L level (GN): Controllable by PAx/PDRx terminals and PBx/MDRx terminals. H level (+V): Uncontrollable by PAx/PDRx terminals and PBx/MDRx terminals.
52	VDD	-	-	-	Power supply terminal. Connects to 3.3 V.
53	P0x/FUPx	B	-	PU (PD)	P0 terminal used for a general purpose I/O port or an output terminal for on-going acceleration signal. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
54	P1x/FDWx	B	-	PU (PD)	P1 terminal used for a general purpose I/O port or an output terminal for on-going slow-down signal. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
55	P2x/MVCx	B	-	PU (PD)	P2 terminal used for a general purpose I/O port or an output terminal for on-going constant speed operation signal. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
56	P3x/CP1x	B	-	PU (PD)	P3 terminal used for a general-purpose I/O port or an output a signal indicating comparator 1 condition is met. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
57	GND	-	-	-	Power supply terminal. Connects to GND.
58	P4x/CP2x	B	-	PU (PD)	P4 terminal used for a general purpose I/O port or output a signal indicating comparator 2 condition is met. See “4.4.4.3 RENV2: Environment setting 2 register” for details.

Terminal No.	Signal name	Direction	Logic	Handling	Description
59	P5x	B	-	PU (PD)	P5 terminal used for a general purpose I/O port See “4.4.4.3 RENV2: Environment setting 2 register” for details.
60	P6x	B	-	PU (PD)	P6 terminal used for a general purpose I/O port See “4.4.4.3 RENV2: Environment setting 2 register” for details.
61	P7x	B	-	PU (PD)	P7 terminal used for a general purpose I/O port See “4.4.4.3 RENV2: Environment setting 2 register” for details.
62	VDD	-	-	-	Power supply terminal Connects to 3.3 V.
63	OUTx	O	N#	OP	Outputs a command pulse to a motor driver. See “7.3.1 Output pulse mode (OUTn, DIRn)” for details.
64	DIRx	O	N#	OP	Outputs a command pulse to a motor driver. See “7.3.1 Output pulse mode (OUTn, DIRn)” for details.
65	ERCx	O	N#	OP	Outputs deviation counter clear signal to a servo motor driver. See “7.5.2 Deviation counter clear signal (ERCn)” for details.
66	BSYx	O	N	OP	Outputs signal to indicate that an operation is busy. It becomes L level during operation.
67	GND	-	-	-	Power supply terminal Connects to GND.
68	PELy	I	N%	+V	Inputs end limit signal on the positive side. See “7.4.1 End limit signal (PELn, MELn)” for details.
69	MELy	I	N%	+V	Inputs end limit signal on the negative side. See “7.4.1 End limit signal (PELn, MELn)” for details.
70	SDy	I	N#	+V	Inputs slow-down signal. See “7.4.2 Slow-down signal (SDn)” for details.
71	ORGy	I	N#	+V	Inputs origin position signal. See “7.4.3 Origin position signal (ORGn), encoder Z-phase signal (EZn)” for details.
72	ALMy	I	N#	+V	Inputs alarm signal input from a servo motor driver. See “7.5.3 Alarm signals (ALMn)” for details.
73	PCSy	I	N#	GN	Inputs pulse count start signal or own-axis start signal. See "7.2.2 Target position override 2 (PCSn)" or "7.6.2 Own-axis start signal (PCSn)" for details.
74	INPy	I	N#	GN	Inputs an in-position signal input from a servo motor driver). See "7.5.1 In-position signal (INPn)” for details.

Terminal No.	Signal name	Direction	Logic	Handling	Description
75	LTCy	I	N#	GN	Input counter latch signals See “7.10.2 Latch and clear (LTCn)” for details.
76	VDD	-	-	-	Power supply terminal. Connects to 3.3 V.
77	EAy	I	-	GN	Inputs A-phase signals from an encoder. See “7.10.1 Counter type and input specification” for details.
78	EBy	I	-	GN	Inputs B-phase signals from an encoder. See “7.10.1 Counter type and input specification” for details.
79	EZy	I	N#	GN	Inputs Z-phase signals from an encoder. See “7.4.3 Origin position signal (ORGn), encoder Z-phase signal (EZn)” for details.
80	PAy/PDRy	I	-	GN	Connects to A-phase of a manual pulser or the positive direction of an external switch. See “5.3 Manual pulser control” or “5.4 Switch control” for details.
81	PBy/MDRy	I	-	GN	Connects to B-phase of a manual pulser or the negative direction of an external switch. See “5.3 Manual pulser control” or “5.4 Switch control” for details.
82	PEy	I	N	GN	Inputs manual pulser signals or external switch enable signals. L level (GN): Controllable by PAy/PDRy terminals and PBy/MDRy terminals. H level (+V): Uncontrollable by PAy/PDRy terminals and PBy/MDRy terminals.
83	GND	-	-	-	Power supply terminal. Connects to GND.
84	P0y/FUPy	B	-	PU (PD)	P0 terminal used for a general purpose I/O port or an output terminal for on-going acceleration signal. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
85	P1y/FDWy	B	-	PU (PD)	P1 terminal used for a general purpose I/O port or an output terminal for on-going slow-down signal. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
86	P2y/MVCy	B	-	PU (PD)	P2 terminal used for a general purpose I/O port or an output terminal for on-going constant speed operation signal. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
87	P3y/CP1y	B	-	PU (PD)	P3 terminal used for a general purpose I/O port or an output terminal for a signal that indicates the condition of comparator 1 is met. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
88	VDD	-	-	-	Power supply terminal. Connects to 3.3 V.
89	P4y/CP2y	B	-	PU (PD)	P4 terminal used for a general purpose I/O port or an output terminal for a signal that indicates the condition of comparator 2 is met. See “4.4.4.3 RENV2: Environment setting 2 register” for details.

Terminal No.	Signal name	Direction	Logic	Handling	Description
90	P5y	B	-	PU (PD)	P5 terminal used for a general purpose I/O port See “4.4.4.3 RENV2: Environment setting 2 register” for details.
91	P6y	B	-	PU (PD)	P6 terminal used for a general purpose I/O port See “4.4.4.3 RENV2: Environment setting 2 register” for details
92	P7y	B	-	PU (PD)	P7 terminal used for a general purpose I/O port See “4.4.4.3 RENV2: Environment setting 2 register” for details.
93	GND	-	-	-	Power supply terminal. Connects to GND.
94	OUTy	O	N#	OP	Outputs command pulses to a motor driver. See “7.3.1 Output pulse mode (OUTn, DIRn)” for details.
95	DIRy	O	N#	OP	Outputs command pulses to a motor driver. See “7.3.1 Output pulse mode (OUTn, DIRn)” for details.
96	ERCy	O	N#	OP	Outputs a deviation counter clear signal to a servo motor driver. See “7.5.2 Deviation counter clear signal (ERCn)” for details.
97	BSYy	O	N	OP	Outputs a signal to indicate that an operation is busy. It becomes to L level during operation.
98	VDD	-	-	-	Power supply terminal. Connects to 3.3 V.
99	PELz	I	N%	+V	Inputs an end limit signal on the positive side. See “7.4.1 End limit signal (PELn, MELn)” for details.
100	MELz	I	N%	+V	Inputs an end limit signal on the negative side. See “7.4.1 End limit signal (PELn, MELn)” for details.
101	SDz	I	N#	+V	Inputs a slow-down signal. See “7.4.2 Slow-down signal (SDn)” for details.
102	ORGz	I	N#	+V	Inputs an origin position signal. See “7.4.3 Origin position signal (ORGn), encoder Z-phase signal (EZn)” for details.
103	ALMz	I	N#	+V	Inputs an alarm signal input from a servo motor driver. See “7.5.3 Alarm signals (ALMn)” for details.
104	PCSz	I	N#	GN	Inputs a pulse count start signal or an own-axis start signal. See “7.2.2 Target position override 2 (PCSn)” or “7.6.2 Own-axis start signal (PCSn)” for details.
105	INPz	I	N#	GN	Inputs an in-position signal from a servo motor driver. See “7.5.1 In-position signal (INPn)” for details.

Terminal No.	Signal name	Direction	Logic	Handling	Description
106	LTCz	I	N#	GN	Input a counter latch signal. See “7.10.2 Latch and clear (LTCn) for details.
107	GND	-	-	-	Power supply terminal. Connects to GND.
108	EAz	I	-	GN	Inputs A-phase signals from an encoder. See “7.10.1 Counter type and input specification” for details.
109	EBz	I	-	GN	Inputs B-phase signals from an encoder. See “7.10.1 Counter type and input specification” for details.
110	EZz	I	N#	GN	Inputs Z-phase signals from an encoder. See “7.4.3 Origin position signal (ORGn), encoder Z-phase signal (EZn)” for details.
111	PAz/PDRz	I	-	GN	Connects to A-phase of a manual pulser or the positive direction of an external switch. See “5.3 Manual pulser control” or “5.4 Switch control” for details.
112	PBz/MDRz	I	-	GN	Connects to B-phase of a manual pulser or the negative direction of an external switch. See “5.3 Manual pulser control” or “5.4 Switch control” for details.
113	PEz	I	N	GN	Inputs manual pulser signals or external switch enable signals. L level (GN): Controllable by PAy/PDRy terminals and PBy/MDRy terminals. H level (+V): Uncontrollable by PAy/PDRy terminals and PBy/MDRy terminals.
114	VDD	-	-	-	Power supply terminal. Connects to 3.3 V.
115	P0z/FUPz	B	-	PU (PD)	P0 terminal used for general purpose I/O port or output terminal for on-going acceleration signal. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
116	P1z/FDWz	B	-	PU (PD)	P1 terminal used for general purpose I/O port or output terminal for on-going slow-down signal. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
117	P2z/MVCz	B	-	PU (PD)	P2 terminal used for general purpose I/O port or output terminal for on-going constant speed operation signal. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
118	P3z/CP1z	B	-	PU (PD)	P3 terminal used for general purpose I/O port or output terminal for signal that indicates the condition of comparator 1 is met. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
119	GND	-	-	-	Power supply terminal. Connects to GND.
120	P4z/CP2z	B	-	PU (PD)	P4 terminal used for general purpose I/O port or output terminal for signal that indicates the condition of comparator 2 is met. See “4.4.4.3 RENV2: Environment setting 2 register” for details.

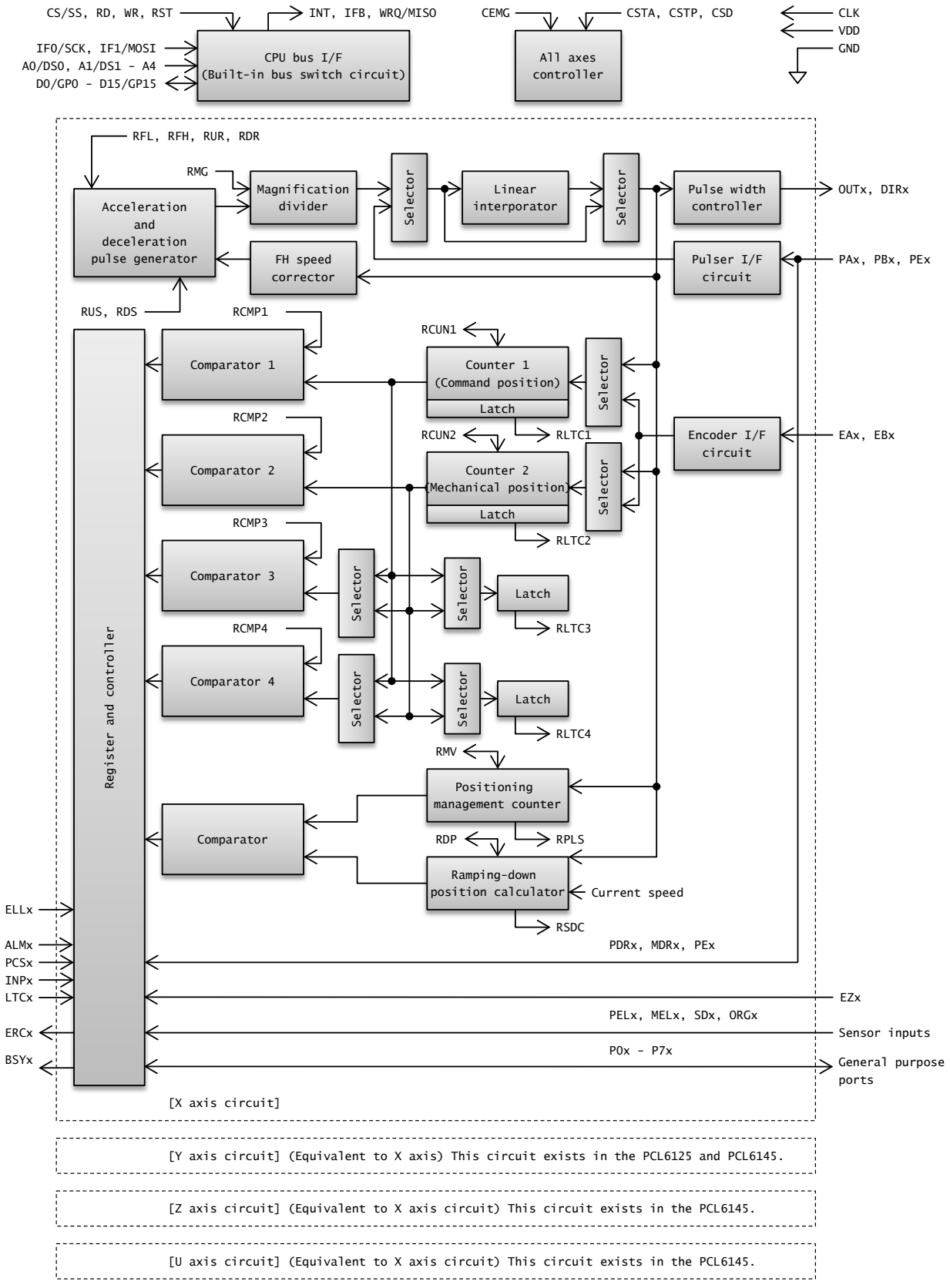
Terminal No.	Signal name	Direction	Logic	Handling	Description
121	P5z	B	-	PU (PD)	P5 terminal used for a general purpose I/O port See “4.4.4.3 RENV2: Environment setting 2 register” for details.
122	P6z	B	-	PU (PD)	P6 terminal used for a general purpose I/O port See “4.4.4.3 RENV2: Environment setting 2 register” for details.
123	P7z	B	-	PU (PD)	P7 terminal used for a general purpose I/O port See “4.4.4.3 RENV2: Environment setting 2 register” for details.
124	VDD	-	-	-	Power supply terminal. Connects to 3.3 V.
125	OUTz	O	N#	OP	Outputs a command pulse to a motor driver. See “7.3.1 Output pulse mode (OUTn, DIRn)” for details.
126	DIRz	O	N#	OP	Outputs a command pulse to a motor driver. See “7.3.1 Output pulse mode (OUTn, DIRn)” for details.
127	ERCz	O	N#	OP	Outputs a deviation counter clear signal to a servo motor driver. See “7.5.2 Deviation counter clear signal (ERCn)” for details.
128	BSYz	O	N	OP	Outputs a signal to indicate that an operation is busy. It becomes L level during the operation.
129	GND	-	-	-	Power supply terminal. Connects to GND.
130	PELu	I	N%	+V	Inputs an end limit signal on the positive side. See “7.4.1 End limit signal (PELn, MELn)” for details.
131	MELu	I	N%	+V	Inputs an end limit signal on the negative side. See “7.4.1 End limit signal (PELn, MELn)” for details.
132	SDu	I	N#	+V	Inputs slow-down signals. See “7.4.2 Slow-down signal (SDn)” for details.
133	ORGu	I	N#	+V	Inputs origin position signals. See “7.4.3 Origin position signal (ORGn), encoder Z-phase signal (EZn)” for details.
134	ALMu	I	N#	+V	Inputs an alarm signal input from a servo motor driver. See “7.5.3 Alarm signals (ALMn)” for details.
135	PCSu	I	N#	GN	Inputs a pulse count start signal or an own-axis start signal. See “7.2.2 Target position override 2 (PCSn)” or “7.6.2 Own-axis start signal (PCSn)” for details.
136	INPu	I	N#	GN	Inputs an in-position signal input from a servo motor driver. See “7.5.1 In-position signal (INPn)” for details.

Terminal No.	Signal name	Direction	Logic	Handling	Description
137	LTCu	I	N#	GN	Input a counter latch signal. See “7.10.2 Latch and clear (LTCn)” for details.
138	VDD	-	-	-	Power supply terminal. Connects to 3.3 V.
139	EAu	I	-	GN	Inputs A-phase signals from an encoder. See “7.10.1 Counter type and input specification” for details.
140	EBu	I	-	GN	Inputs B-phase signals from an encoder. See “7.10.1 Counter type and input specification” for details.
141	EZu	I	N#	GN	Inputs Z-phase signals from an encoder. See “7.4.3 Origin position signal (ORGn), encoder Z-phase signal (EZn)” for details.
142	PAu/PDRu	I	-	GN	Connects to A-phase of a manual pulser or the positive direction of an external switch. See “5.3 Manual pulser control” or “5.4 Switch control” for details.
143	PBu/MDRu	I	-	GN	Connects to B-phase of a manual pulser or the negative direction of an external switch. See “5.3 Manual pulser control” or “5.4 Switch control” for details.
144	PEu	I	N	GN	Inputs manual pulser signals or external switch enable signals. L level (GN): Controllable by PAy/PDRy terminals and PBy/MDRy terminals. H level (+V): Uncontrollable by PAy/PDRy terminals and PBy/MDRy terminals.
145	GND	-	-	-	Power supply terminal. Connects to GND
146	P0u/FUPu	B	-	PU (PD)	P0 terminal used for a general purpose I/O port or an output terminal for on-going acceleration signals. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
147	P1u/FDWu	B	-	PU (PD)	P1 terminal used for a general purpose I/O port or an output terminal for on-going slow-down signals. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
148	P2u/MVCu	B	-	PU (PD)	P2 terminal used for a general purpose I/O port or an output terminal for on-going constant speed operation signals. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
149	P3u/CP1u	B	-	PU (PD)	P3 terminal used for a general purpose I/O port or an output terminal for signal that indicates the condition of comparator 1 is met. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
150	VDD	-	-	-	Power supply terminal. Connects to 3.3 V.

Terminal No.	Signal name	Direction	Logic	Handling	Description
151	P4u/CP2u	B		PU	P4 terminal used for a general purpose I/O port or an output terminal for a signal that indicates the condition of comparator 2 is met. See “4.4.4.3 RENV2: Environment setting 2 register” for details.
152	P5u	B	-	PU (PD)	P5 terminal used for a general purpose I/O port See “4.4.4.3 RENV2: Environment setting 2 register” for details.
153	P6u	B	-	PU (PD)	P6 terminal used for a general purpose I/O port See “4.4.4.3 RENV2: Environment setting 2 register” for details
154	P7u	B	-	PU (PD)	P7 terminal used for a general purpose I/O port See “04.4.4.3 RENV2: Environment setting 2 register” for details.
155	GND	-	-	-	Power supply terminal Connects to GND.
156	OUTu	O	N#	OP	Outputs a command pulse to a motor driver. See “7.3.1 Output pulse mode (OUTn, DIRn)” for details.
157	DIRu	O	N#	OP	Outputs a command pulse to a motor driver. See “7.3.1 Output pulse mode (OUTn, DIRn)” for details.
158	ERCu	O	N#	OP	Outputs a deviation counter clear signal to a servo motor driver. See “7.5.2 Deviation counter clear signal (ERCn)” for details.
159	BSYu	O	N	OP	Outputs a signal to indicate that an operation is busy. It becomes to L level during operation.
160	VDD	-	-	-	Power supply terminal. Connects to 3.3 V.
161	(GND)	I	-	GN	Input terminal for shipping inspection. Connects to GND.
162	GND	-	-	-	Power supply terminal. Connects to GND.
163	CLK	I	-	-	Inputs reference clock (CLK) signal. Standard frequency is 19.6608 MHz.
164	VDD	-	-	-	Power supply terminal. Connects to GND.
165 166	(GND)	I	-	GN	Input terminal for shipping inspection. Connects to GND.
167	CSD	B	N	PU	Inputs and outputs simultaneous slow-down signals. See “7.7.1 Simultaneous slow-down signal (CSD)” for details.

Terminal No.	Signal name	Direction	Logic	Handling	Description
168	CSTA	B	N	PU	Inputs/outputs a simultaneous start signal. See “7.6.1 Simultaneous start signal (CSTA)” for details.
169	CSTP	B	N	PU	Inputs/outputs a simultaneous stop signal. See “7.8.1 Simultaneous stop signal (CSTP)” for details.
170	CEMG	I	N	+V	Inputs an emergency stop signal. See “7.9.1 Emergency stop signal (CEMG)” for details.
171	ELLx	I	-	-	Selects the input logic of end limit signal. L level (GN): Input logic is positive. H level (+V): Input logic is negative.
172	ELLy	I	-	-	Selects the input logic for an end limit signal. L level (GN): Input logic is positive. H level (+V): Input logic is negative.
173	ELLz	I	-	-	Selects the input logic of an end limit signal. L level (GN): Input logic is positive. H level (+V): Input logic is negative.
174	ELLu	I	-	-	Selects the input logic for an end limit signal. L level (GN): Input logic is positive. H level (+V): Input logic is negative.
175	RST	I	N	-	Inputs a reset signal. See “7.1 Reset” for details.
176	GND	-	-	-	Power supply terminal Connects to GND.

3.4 Block Diagram



3.5 CPU bus interface

This LSI contains a total of 5 types of interface circuit: 4 types of parallel bus interface circuit and 1 type of serial bus interface circuit, making it easier to connect to a variety of CPUs.

3.5.1 Parallel bus interface

This section explains the CPU settings and the CPU connections when the parallel bus interface is selected.

3.5.1.1 CPU settings

If either RD terminal or WR terminal is at H level at the rising edge of a reset signal, it becomes parallel bus interface.

Parallel bus interface circuit is selected by IF0 and IF1 terminals.

If a selected CPU is not in the following list, select the most suitable interface circuit.

Please see “8.4 AC characteristics” for the detail.

[Examples of parallel bus interface CPU signal connections]

Setting status		Interface name	CPU type	CPU signal to connect			
IF1	IF0			RD terminal	WR terminal	A0 terminal	WRQ terminal
L	L	16-bit interface-1	68000	+3.3 V	R/W	LDS	DTACK
L	H	16-bit interface-2	H8	RD	HWR	(GND)	WAIT
H	L	16-bit interface-3	8086	RD	WR	(GND)	READY
H	H	8-bit interface	Z80	RD	WR	A0	WAIT

16-bit interface-1: 16-bit interface with R/W signal, LDS signal and DTACK signal.
The lower addresses correspond to the upper word in I/O buffer.
This interface is easy to use with VME bus and 68000 series CPUs.

16-bit interface-2: 16-bit interface with RD signal, HWR signal and WAIT signal.
The lower addresses correspond to the upper word in I/O buffer.
This interface is easy to use with H8 series CPUs.

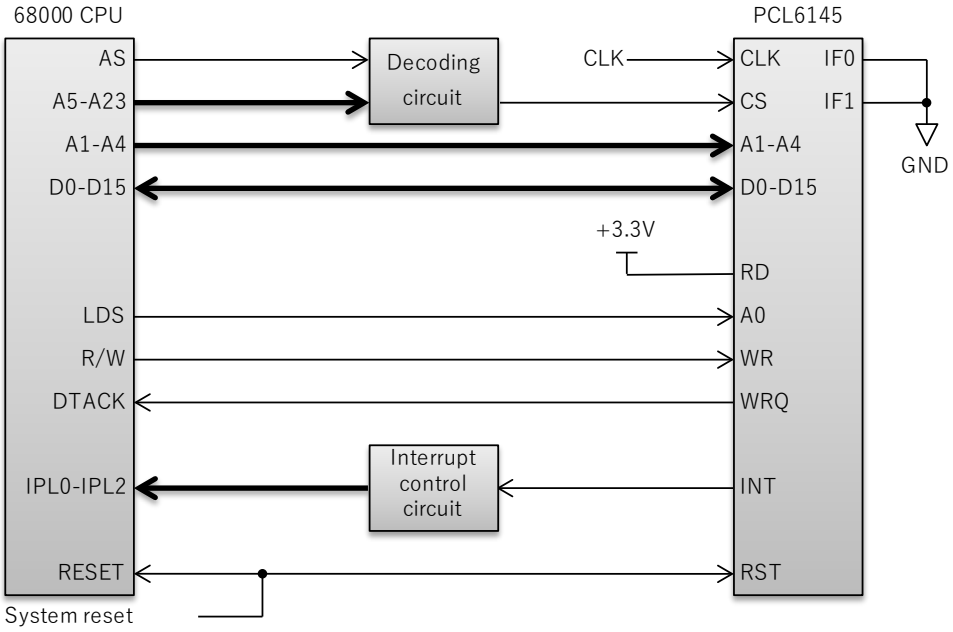
16-bit interface-3: 16-bit interface with RD signal, WR signal and WAIT signal.
The lower addresses correspond to the lower word in I/O buffer.
This interface is easy to use with 8086 series CPUs.

8-bit interface: 8-bit interface with RD signal, WR signal and WAIT signal.
The lower addresses correspond to the lower word in I/O buffer.
This interface is easy to use with Z80 series CPUs.

3.5.1.2 Examples of CPU connection

3.5.1.2.1 16-bit interface-1

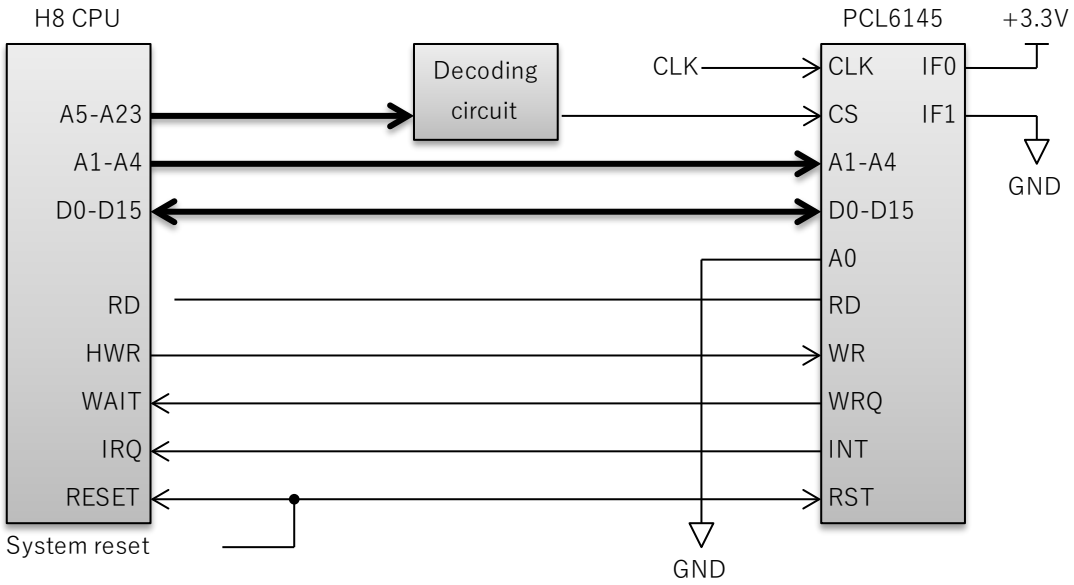
Setting status to select CPU bus interface: “IF1 terminal = L level” and “IF0 terminal = L level”.



Note:
1. Connects A0 to LDS for all LSI models.
2. The following terminals are connected to the addresses of CPU.
   PCL6145: A1 to A4, PCL6125: A1 to A3, PCL6115: A1 and A2.
3. For 16-bit interface, word-size-access (16-bit) is available, but byte-size-access (8-bit) is not available.

3.5.1.2.2 16-bit interface-2

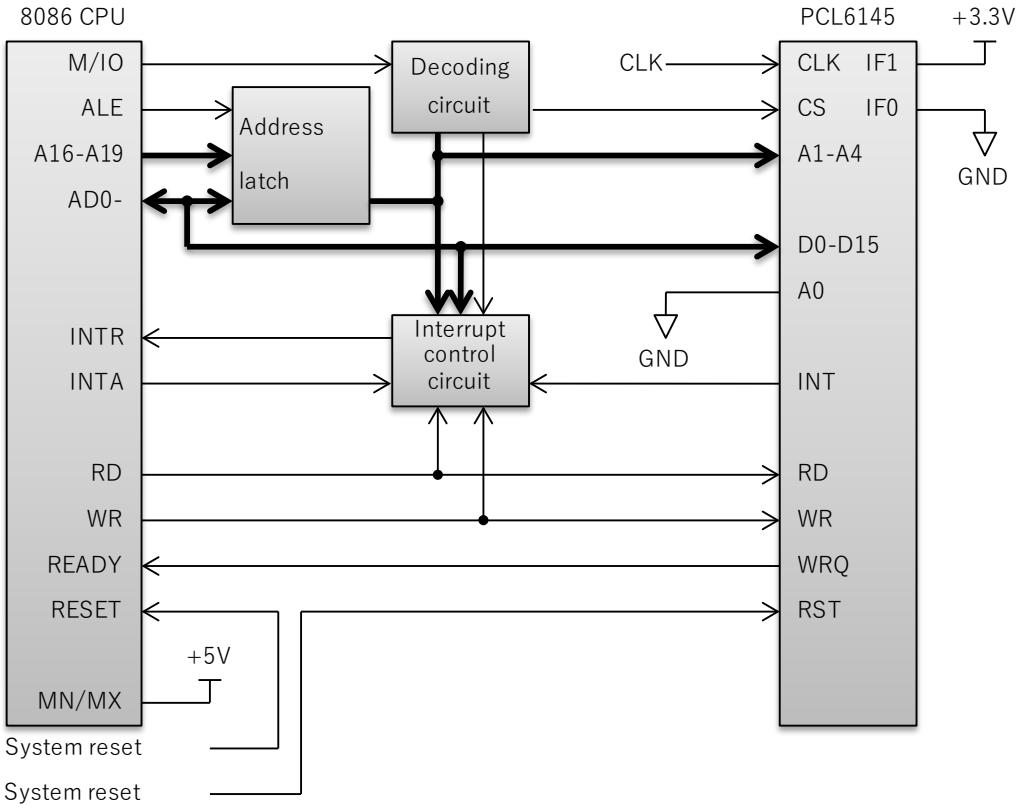
Setting status to select CPU bus interface: “IF1 terminal = L level” and “IF0 terminal = H level”.



Note:
1. Connects A0 to GND for all LSI models.
2. The following terminals are connected to the addresses of CPU.
3. PCL6145: A1 to A4, PCL6125: A1 to A3, PCL6115: A1 and A2.
4. For 16-bit interface, word-size-access (16-bit) is available, but byte-size-access (8-bit) is not available.

3.5.1.2.3 16-bit interface-3

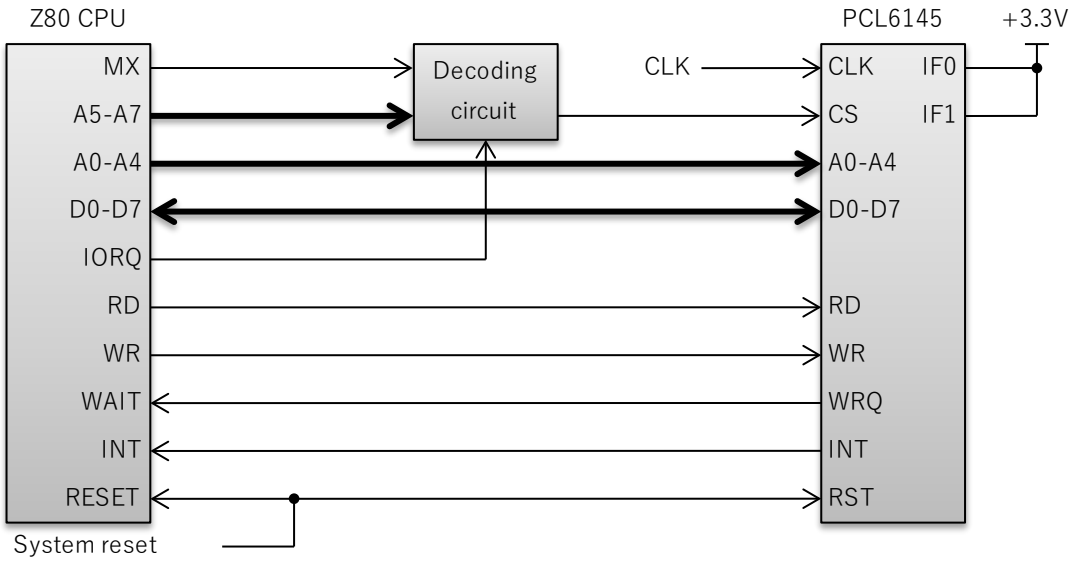
Setting status to select CPU bus interface: “IF1 terminal = H level” and “IF0 terminal = L level”.



Note:
1. Connects A0 to GND for all LSI models.
2. The following terminals are connected to the addresses of CPU:
   PCL6145: A1 to A4, PCL6125: A1 to A3, PCL6115: A1 and A2.
3. For 16-bit interface, word-size-access (16-bit) is available, but byte-size-access (8-bit) is not available.

3.5.1.2.4 8-bit interface

Setting status to select CPU bus interface: “IF1 terminal = H level” and “IF0 terminal = H level”.



Note: The following terminals are connected to the addresses of CPU.
PCL6145: A1 to A4, PCL6125: A1 to A3, PCL6115: A1 and A2.

3.5.2 Serial bus interface

In this chapter, we will explain CPU settings and CPU connections when a serial bus interface is selected.

3.5.2.1 Connecting CPU settings

When both RD terminal and WR terminal are in L level at the rising edge of reset signal, it becomes parallel bus interface.

[Example of serial bus interface CPU signal connection]

Settings		Interface name	Connecting CPU signal			
RD	WR		IF0 terminal	IF1 terminal	CS terminal	WRQ terminal
L	L	Serial bus interface	SCK	MOSI	SS	MISO
Other than the above.		Parallel bus interface	See “3.5.1.1 CPU settings”.			

Serial bus interface :4-wire synchronous type serial bus interface is built-in.
Extended connection up to 4 LSIs is available with one slave select signal (SS).
LSIs that are extended in connection can be identifed by device selection information set in DS0 and DS1 terminals.

SCK (Serial Clock):Clock terminal for serial bus interface.

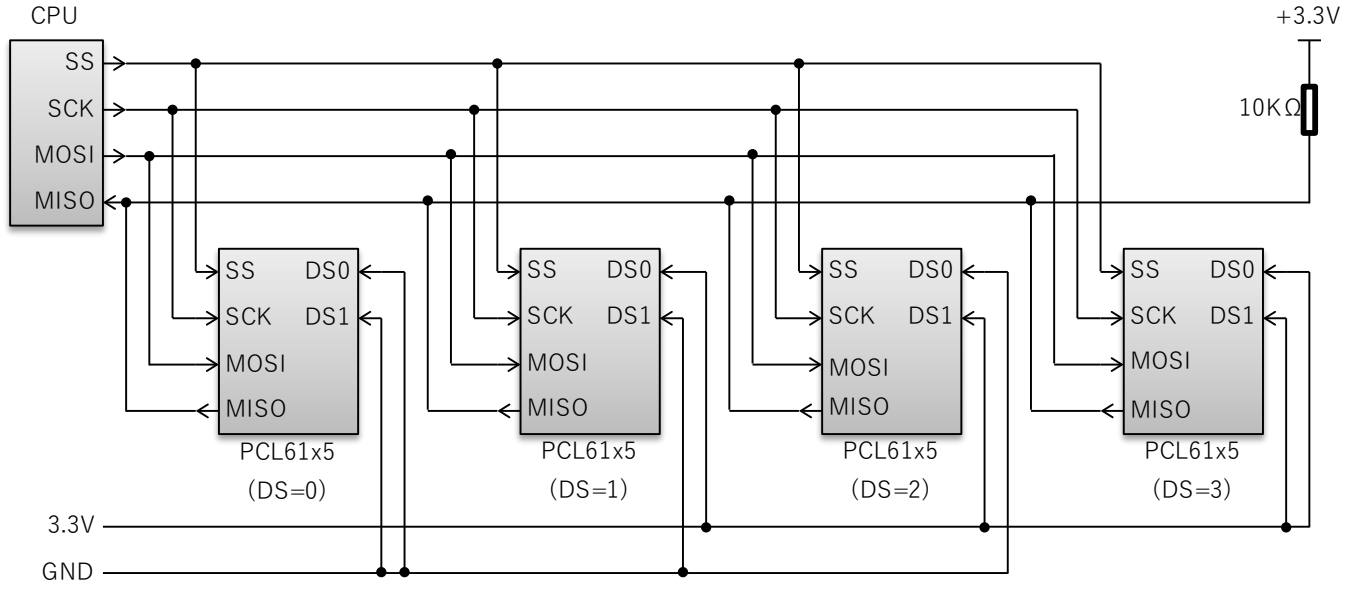
SS (Slave Select):Input terminal for slave (LSI) selection.

MOSI (Master Output Slave Input):Input terminal from the master (CPU) to the slave (LSI).

MISO (Master Input Slave Output):Output terminal from the slave (LSI) to the master (CPU).

3.5.2.2 Example of CPU bus interface connection

Setting status to select CPU bus interface: “RD = L level” and “WR = L level”.



Note: The pull-up resistor is connected to prevent CPU and PCL61×5 from being damaged when floating.

4. Software description

This section explains the software such as CPU access and commands.

4.1 CPU access

There are two communiation types:

1) parallel communication used for parallel bus interface

2) serial communication used for serial bus interface.

4.1.1 Parallel communication

Address map and access method used for parallel communication are shown as follows.

4.1.1.1 Address map

Address map for parallel communication includes “Axis arrangement map” and “Axis internal map” as follows:

4.1.1.1.1 Axis arrangement map

In this LSI, the control address range for each axis is independent. It is selected by using address input terminal; A4 and A3 as follows.

A4	A3	Detail	LSI
0	0	X-axis control address range	PCL6145, PCL6125 (A3 terminal only), PCL6115 (without A3 and A4 terminals)
0	1	Y-axis control address range	PCL6145, PCL6125(A3 terminal only)
1	0	Z-axis control address range	PCL6145
1	1	U-axis control address range	PCL6145

4.1.1.1.2 Axis internal map

The axis internal map is defined by address inputs A2, A1 (, and A0).

4.1.1.1.2.1 16-bit interface-1 or 16-bit interface-2

1) Write cycle

A2	A1	Name	Processing description
0	0	BUFW1	Write to I/O buffer (bits 31 to 16)
0	1	BUFW0	Write to I/O buffer (bits 15 to 0).
1	0	OTPW	Change statuses of general-purpose output ports (only the bits assigned as outputs are enabled).
1	1	COMW	Write axis selections and commands.

2) Read cycle

A2	A1	Address name	Processing description
0	0	BUFW1	Read from I/O buffer (bits 31 to 16).
0	1	BUFW0	Read from I/O buffer (bits 15 to 0).
1	0	SSTSW	Read sub status and general-purpose I/O ports.
1	1	MSTSW	Read main-status (bits 15 to 0).

4.1.1.1.2.2 16-bit interface-3

1) Write cycle

A2	A1	Address name	Processing description
0	0	COMW	Write axis selections and commands.
0	1	OTPW	Change statuses of general-purpose output ports (only the bits assigned as outputs are enabled)
1	0	BUFW0	Write to I/O buffer (bits 15 to 0)
1	1	BUFW1	Write to I/O buffer (bits 31 to 16)

2) Read cycle

A2	A1	Address name	Processing description
0	0	MSTSW	Read main-status (bits 15 to 0)
0	1	SSTSW	Read sub status and general-purpose I/O port
1	0	BUFW0	Read from I/O buffer (bits 15 to 0)
1	1	BUFW1	Read from I/O buffer (bits 31 to 16)

4.1.1.1.2.3 8-bit interface

1) Write cycle

A2	A1	A0	Address name	Processing description
0	0	0	COMB0	Write commands
0	0	1	COMB1	Write axis selection (specify the axis to execute a command)
0	1	0	OTPB	Change statuses of general-purpose output ports (only the bits assigned as outputs are enabled)
0	1	1	-	(Not available)
1	0	0	BUFB0	Write to I/O buffer (bits 7 to 0)
1	0	1	BUFB1	Write to I/O buffer (bits 15 to 8)
1	1	0	BUFB2	Write to I/O buffer (bits 23 to 16)
1	1	1	BUFB3	Write to I/O buffer (bits 31 to 24)

2) Read cycle

A2	A1	A0	Address name	Processing description
0	0	0	MSTSB0	Read main-status (bits 7 to 0)
0	0	1	MSTSB1	Read main-status (bits 15 to 8)
0	1	0	IOPB	Read general-purpose I/O ports
0	1	1	SSTSB	Read sub status
1	0	0	BUFB0	Read from I/O buffer (bits 7 to 0)
1	0	1	BUFB1	Read from I/O buffer (bits 15 to 8)
1	1	0	BUFB2	Read from I/O buffer (bits 23 to 16)
1	1	1	BUFB3	Read from I/O buffer (bits 31 to 24)

4.1.1.2 How to access

Wrting commands, writing registers, reading registers, reading main-statuses, writing general-purpose output ports, and reading sub statuses & general-purpose I/O ports can be done using the address map.

4.1.1.2.1 Writing commands

4.1.1.2.1.1 Axis selections, Commands

Write “Axis selections” and “Command codes” in COMW addresses.

COMW															
COMB1								COMB0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	SELu	SELz	SELy	SELx	COM							

COMW.COMB1: Set “Axis selection codes”.
Write commands to the axis that “1” is set from SELx to SELu.
If “1” is set for multiple bits, the same command can be written to multiple axes that are selected.
When “0” are set all from SELx to SELu, only the own-axis (axis selected by A4 and A3 terminals) is selected.

COMW.COMB0: Set “Command codes”.
See “4.3 Commands” for details.

Note:

1: Settings from SELx to SELu are effective for all commands.

2: PCL6145 can select from SELx to SELu; PCL6125 can select SELx and SELy.
However, PCL6115 ignores writing to COMB1 address.

For 8-bit interface, write “command codes” to COMB 0 address after writing “axis selection code” to COMB 1 address.

For 16-bit interface, write 16-bit data including “axis selection code” and “command code” to COMW address.

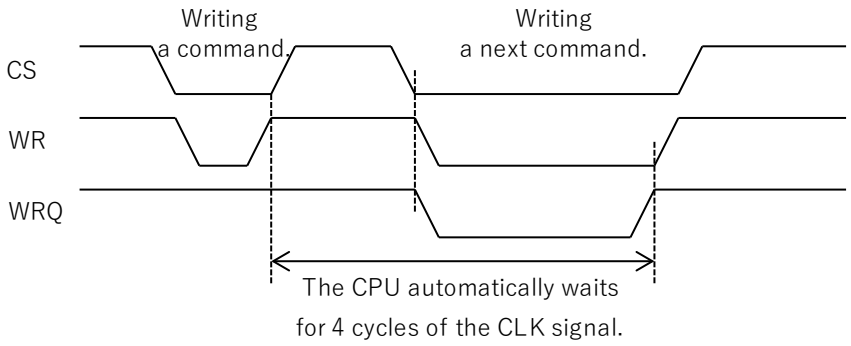
4.1.1.2.1.2 Writing procedures

When writing commands consecutively, waiting time of 4 reference clock frequency cycles (approximately 0.2 µs) is required between commands.

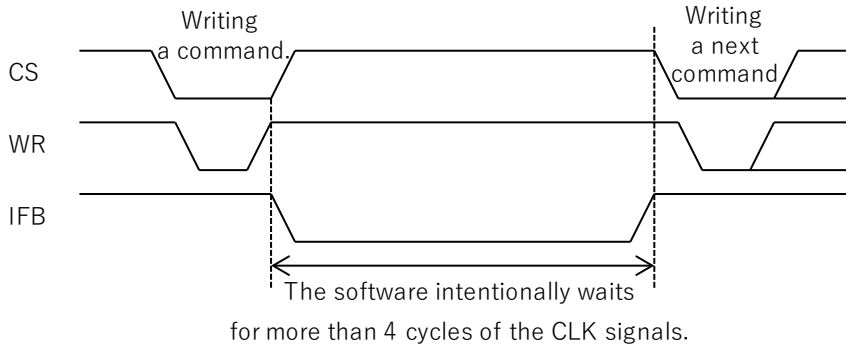
When WRQ signal is available with CPU, the CPU automatically secures the waiting time.

When WRQ signal is not available with CPU, make sure to secure this waiting time of 4 reference clock frequency cycles or longer with software.

1. When WRQ signal is used (16-bit interface)



2. When WRQ signal is not used (16-bit interface)



Note:

1. While CS signal and IFB signal are both at L level, WRQ signal goes to L level.
2. When WRQ signal is not used, it is recomanded to access after making sure of “IFB = H level”.

4.1.1.2.2 Writing registers

4.1.1.2.2.1 I/O buffer (BUF)

"Data to write to the registers", is written to BUFW0 and BUFW1 addresses.

BUFW1																BUFW0															
BUFB3								BUFB2								BUFB1								BUFB0							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUF																															

BUFW1 (BUFB3, BUFB2): Set the upper data.

BUFW0 (BUFB1, BUFB0): Set the lower data.

Write "register writing data" to I/O buffers.

When the "register writing command" is wirtten to COMW address, it will be copied from the I/O buffer to the register.

The order of writing to I/O buffer (BUFW 0, 1) is arbirary.

Also, the contents written to I/O buffer can be read.

There are two ways to write "register data" as follows:

They can be combined to use since they are just ideas on software designing.

The following is an example using PCL6145.

1. Consider writing commands and I/O buffers as one set and use four sets of areas totally.
   In this case, axis selection (COMB 1) can be used at 00h.
   Then using multiple LSIs, it is easier to create a common program.
   e.g. 16-bit interface-3

A4 to A1	Address name	Description
0000	COMW_X	X-axis command
0010	BUFW0_X	X-axis I/O buffer (Bits 15 to 0)
0011	BUFW1_X	X-axis I/O buffer (Bits 31 to 16)
0100	COMW_Y	Y-axis command
0110	BUFW0_Y	Y-axis I/O buffer (Bits 15 to 0)
0111	BUFW1_Y	Y-axis I/O buffer (Bits 31 to 16)
1000	COMW_Z	Z-axis command
1010	BUFW0_Z	Z-axis I/O buffer (Bits 15 to 0)
1011	BUFW1_Z	Z-axis I/O buffer (Bits 31 to 16)
1100	COMW_U	U-axis command
1110	BUFW0_U	U-axis I/O buffer (Bits 15 to 0)
1111	BUFW1_U	U- axis I/O buffer (Bits 31 to 16)

2. Writing commands is conducted in the common area; only writing I/O buffer is conducted in individual area of each axis.
   So, the axis needs to be selected when writing all commands.
   Since data is written to the same registers of axes selected by one command at one time, the data setting time can be shortened.

e.g. 16-bit interface-3

A4 to A1	Address name	Description
0000	COMW	Axis selection, command
0010	BUFW0_X	X- axis I/O buffer (Bits 15 to 0)
0011	BUFW1_X	X- axis I/O buffer (Bits 31 to 16)
0110	BUFW0_Y	Y- axis I/O buffer (Bits 15 to 0)
0111	BUFW1_Y	Y- axis I/O buffer (Bits 31 to 16)
1010	BUFW0_Z	Z- axis I/O buffer (Bits 15 to 0)
1011	BUFW1_Z	Z- axis I/O buffer (Bits 31 to 16)
1110	BUFW0_U	U- axis I/O buffer (Bits 15 to 0)
1111	BUFW1_U	U- axis I/O buffer (Bits 31 to 16)

Note: In the above example, COMW address on X-axis is used, but the same result is obtained using COMW address of any axis.

4.1.1.2.2.2 Axis selection, Commands

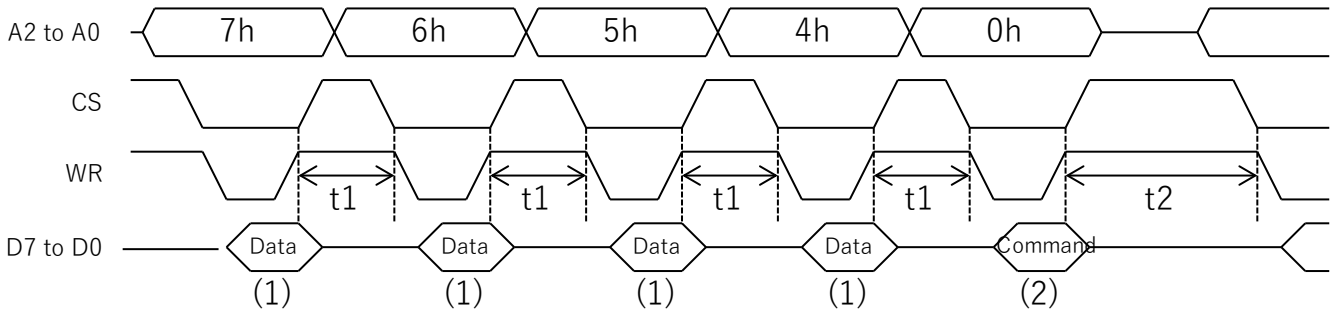
See “4.1.1.2.1.1 Axis selections, commands” for details.

4.1.1.2.2.3 Writing procedures

1) Write “register data” to BUFB3, BUFB2, BUFB1, BUFB0 addresses.
   Writing order is arbitrary. Be sure for the waiting time (t1); 2 cycles of CLK signal (0.1 μs) or longer.
2) Write “register commands” to COMW address.
   When writing the next data and command consecutively, a waiting time(t2) of 4 reference clock frequency cycles (0.2 μs) is required.

In both t1 and t2, if WRQ signal can be used by CPU, the waiting time is automatically secured by CPU.

e.g. 8-bit interface (Axis selection is omitted.)



4.1.1.2.3 Reading registers

4.1.1.2.3.1 I/O buffer (BUF)

"Register data" is read from BUFW0 and BUFW1 addresses.

BUFW1								BUFW0							
BUFB3				BUFB2				BUFB1				BUFB0			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUF																															

BUFW1 (BUFB3, BUFB2): Obtain the upper data.

BUFW0 (BUFB1, BUFB0): Obtain the lower data.

"Register data" is read from I/O buffer.

When "register reading command" is written to COMW address, the data will be copied from register to I/O buffer.

There is no order to read from I/O buffer (BUFW0, 1).

4.1.1.2.3.2 Axis selections, Command

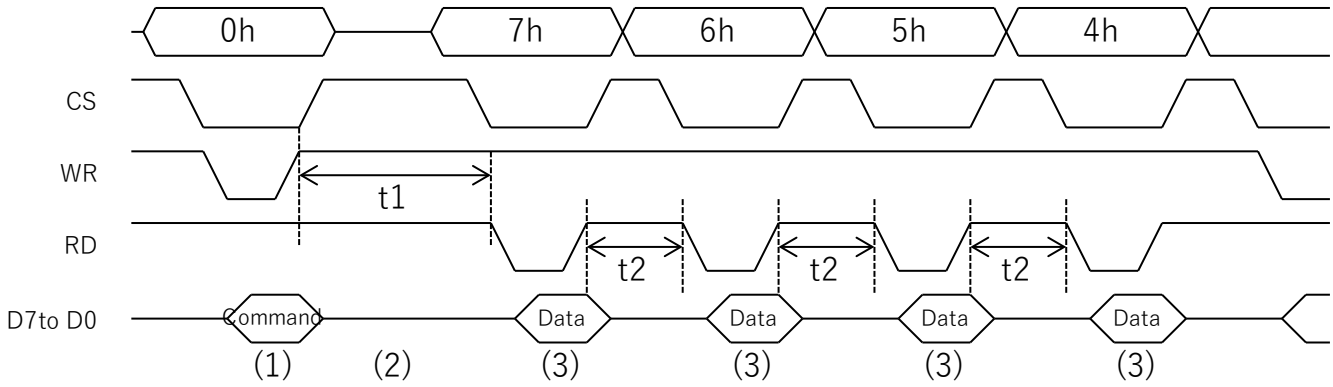
See "4.1.1.2.1.1 Axis selections, Commands" for details.

4.1.1.2.3.3 Reading procedures

1) Write "register reading command" to COMB0 address.
2) Wait until "register reading data" is copied to BUFB3, BUFB2, BUFB1, and BUFB0 address. A waiting time (t1); 4 cycles of CLK signal (0.2 µs) or longer is required.
3) Read "register reading data" from BUFB3, BUFB2, BUFB1, BUFB0 addresses. Reading order is arbitrary. There is no limitation on a wait time for reading (t2).

If WRQ signal can be used by CPU, the waiting time is automatically secured by CPU.

e.g. 8-bit interface (Axis selection is omitted.)



4.1.1.2.4 Reading main-status

4.1.1.2.4.1 Main-status(MSTS)

"Main-status"(MSTS) is read from MSTSW address.

MSTSW															
MSTSB1								MSTSB0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSTS															

MSTSW (MSTSB1, MSTSB0): "MSTS" is obtained.

For the detais of "MSTS", see "4.2.1 Main-status (MSTS)".

4.1.1.2.4.2 Reading procedures

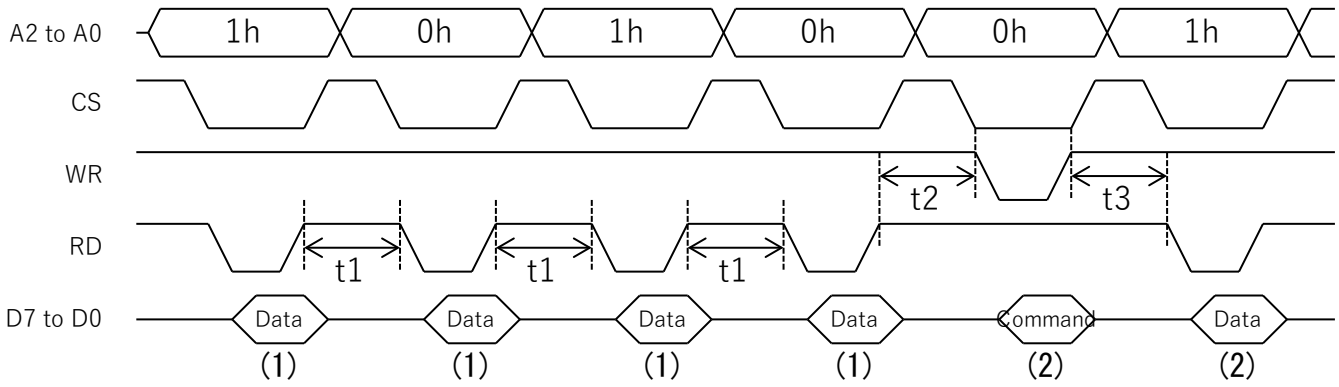
1) Read "MSTS" from MSTSB1, MSTSB0 addresses.

   No particular order for reading. There is no limitation on a wait time for reading (t1).

2) There is no limit to a wait time (t2) to write commands after reading "MSTS", and a wait time (t3) to read "MSTS" after writing commands.

   The main-status during parallel communication is updated by inputting CLK signal once or more while "RD = H level".

e.g. 8-bit interface (Axis selection is omitted.)



4.1.1.2.5 Writing general-purpose output ports

4.1.1.2.5.1 General-purpose output port (OTP)

"General-purpose output port"(OTP) is written to OTPW address.

OTPW															
-								OTPB							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	OTP							

OTPW.OTPB: Sets "OTP".
Set the status of general-purpose I/O terminals (P7 to P0) that have been specified to be output.
H level is output when "1" is set
Settings to the general-purpose I/O terminals that have been set to input will be ignored.

For 16-bit interface, set "0" to the upper 8-bits.

See "4.2.2 Sub status (SSTS) and general-purpose I/O ports (IOP)" for details.

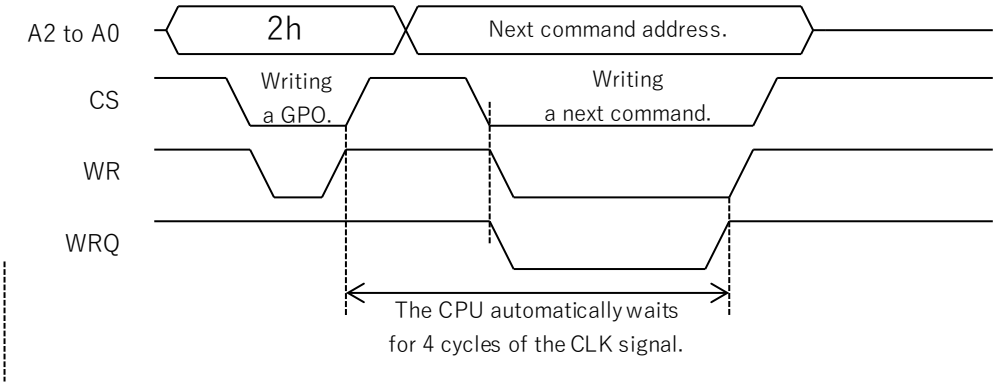
4.1.1.2.5.2 Writing procedure

When writing commands and "OTP" continuously, it is necessary to wait for 4 clock cycles (0.2 µs).

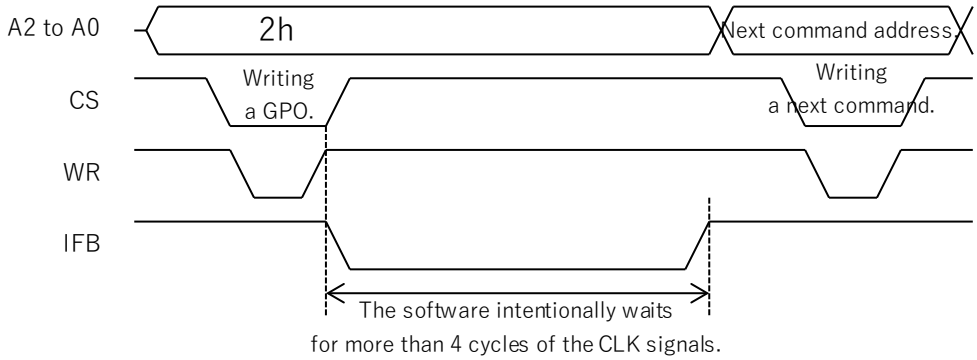
If WRQ signal can be used by CPU, a wait time is automatically secured.

If WRQ signal cannot be used by CPU, secure a wait time; 4 cycles or more of CLK signal by software.

1. When WRQ signal is used (16-bit interface)



2. When WRQ signal is not used (16-bit interface)



Note:

1. While both CS signal and IFB signal are at L level, WRQ signal goes to L level.
2. When WRQ signal is not used, it is recommended to check "IFB = H level" before accessing.

4.1.1.2.6 Reading sub status and general-purpose I/O ports

4.1.1.2.6.1 Sub-status (SSTS) and general-purpose I/O port(IOP)

Sub-status (SSTS) and general purpose I/O port (IOP) are read from SSTSW address.

SSTSW															
SSTSB								IOPB							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSTS								IOP							

SSTSW.SSTSB: “SSTS” is obtained.

SSTSW.IOPB: “IOP” is obtained.

On “SSTS” and “IOP”, see “4.2.2 Sub status (SSTS) and general-purpose I/O ports (IOP)”.

4.1.1.2.6.2 Reading procedures

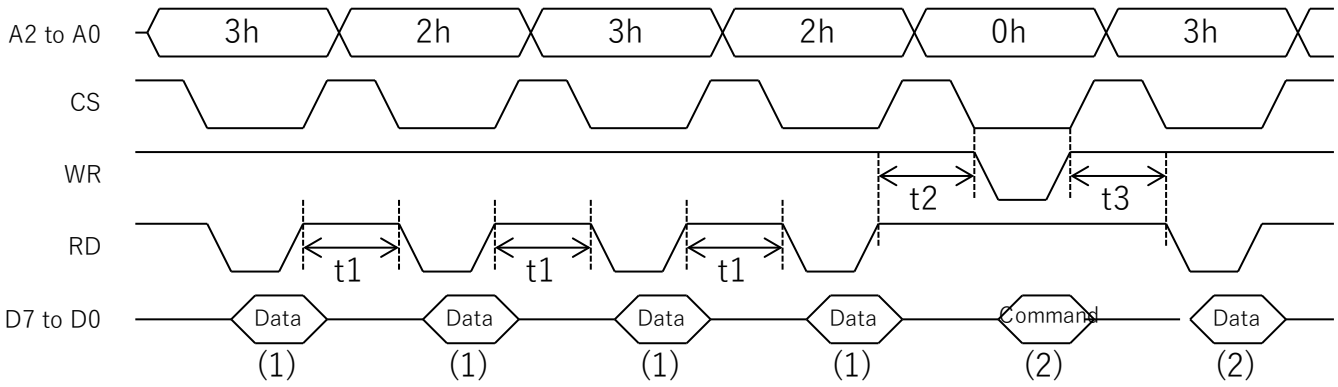
1) Read “SSTS” and “IOP” from SSTSB, IOPB address.

   No particular order for reading. There is not limitation on a wait time for reading (t1).

2) There is no limitation on the wait time (t2) to write commands after reading "SSTS" and “IOP” and the wait time (t3) to read "SSTS" and “IOP” after writing commands.

   Sub status during parallel communication is updated by inputting CLK signal once or more while "RD = H level".

e.g. 8-bit interface (Axis selection is ommited.)



4.1.2 Serial communication

The format of serial communication and the access method are as follows.

4.1.2.1 Communication format

The writing format (MOSI) consists of “Axis selection (SEL)”, “Command (COM)” and “Data (DAT)”.

“Axis selection (SEL)” must be included.

“Commands (COM)” and “Data (DAT)” may not be included depending on the access method.

The numbers of “data (DAT)” are different depending on “axis selections (SEL)”, and the lengths are different depending on the access methods.

<When the number of data is the largest and the is the longest >

MOSI:	SEL	COM	DATx	DATy	DATz	DATu
	S7 to S0	C7 to C0	D31x to D0x	D31y to D0y	D31z to D0z	D31u to D0u

The read format (MISO) consists only of “data (DAT)”. “Data (DAT)” size is different depending on the access method

< When the number of data is the largest and the data length is the longest >

MISO:	DATx	DATy	DATz	DATu
	D31x to D0x	D31y to D0y	D31z to D0z	D31u to D0u

4.1.2.1.1 Axis selection (SEL)

It consists of “Axis selection code”, “Type selection code” and “Device selection code”.

SEL							
S7	S6	S5	S4	S3	S2	S1	S0
Device selection code		Type selection code		Axis selection code			

SEL.S7, S6: Sets “Device selection code”.
Communication is established with the LSI whose device selection number matches the value of “Device selection code”.
The device selection number is the set value in DS1 and DS0 terminals.
By using the device selection number, up to 4 LSIs can be connected with one SS signal.

Device selection code		Device selection number	
SEL.S7	SEL.S6	DS1 terminal	DS0 terminal
0	0	L	L
0	1	L	H
1	0	H	L
1	1	H	H

SEL.S5, S4: Sets “Type selection code”
Select from 4 types of communication format.

Type selection code		Communication format
SEL.S5	SEL.S4	
0	0	Write commands (including register writing and reading).
0	1	Read main-status
1	0	Write general-purpose output port
1	1	Read sub status and general-purpose I/O port

SEL.S3 to S0: Set “Axis selection codes”.
Write commands to the axis that “1” is set from SELu to SELx.

If “1” is set for multiple bits, the same command can be written to the selected axes.
If “0” is set for all axes, it is assumed that only X-axis is selected.

LSI	Axis selection code			
	S3	S2	S1	S0
PCL6145	SELu	SELz	SELy	SELx
PCL6125	0	0	SELy	SELx
PCL6115	0	0	0	SELx

4.1.2.1.2 Commands(COM)

It consists only of “Command code”.

COM							
C7	C6	C5	C4	C3	C2	C1	C0
Command code							

See “4.3 Commands” for details.

4.1.2.1.3 Data (DAT)

It consists of various numbers of “data” depending on the axis selection code.

The selected axes are arranged by X, Y, Z, and U order.

(The following shows an example)

SEL=0001b:	DATx			
SEL=0110b:	DATy	DATz		
SEL=1011b:	DATx	DATy	DATu	
SEL=1111b:	DATx	DATy	DATz	DATu

Also, it consists of “data” of various lengths depending on the access method (type selection code).

DATn			
D7 to D0	D15 to D8	D23 to D16	D31 to D24
Register writing data			
Register reading data			
Main-status reading data		-	
General-purpose output port write data	-		
General-purpose output port read data	Sub status read data	-	

<Register writing data>

They are arranged from X-axis to U-axis in 4-byte unit.

Each axis is arranged from low byte to high byte.

If writing data is less than 4 bytes, 00h is required for the insufficient byte. (12345h → 45h, 23h, 01h, 00h)

Each byte is arranged from MSB to LSB.

If writing data is less than 8 bits, 0b is required for the insufficient bit. (67h → 1100111b → 01100111b)

<Register reading data>

They are arranged from X axis to U-axis in 4-byte unit.

Each axis is arranged from low byte to high byte.

Each byte is arranged from MSB to LSB.

<Main-status reading data>

They are arranged from X-axis to U-axis in 2-byte units.

Each axis is arranged from low byte to high byte.

Each byte is arranged from MSB to LSB.

<General-purpose output port writing data>

They are arranged from X-axis to U-axis in 1-byte units.

Each byte is arranged from MSB to LSB.

If writing data is less than 8 bits, 0b is required for the insufficient bit. (67h → 1100111b → 01100111b)

<Sub-status and general-purpose I/O port read data>

They are arranged from X-axis to U-axis in 2-byte units.

Each axis is arranged from low byte to high byte.

Each byte is arranged from MSB to LSB.

4.1.2.2 Access method

Writing commands, writing registers, reading registers, reading main-statuses, writing general-purpose output ports, and reading sub statuses & general-purpose I/O ports can be done using communication format.

Note:

1. If you interrupt control (SS signal becomes H level in the middle of writing) without writing the number of bits as specified in format, unexpected data is written.
2. If you interrupt control (SS signal becomes H level in the middle of reading) without finish reading the number of bits as specified in format, the remaining data is destroyed.

4.1.2.2.1 Writing commands

4.1.2.2.1.1 Axis selection, command

Write “Axis selection” and “Commands” by writing command format.

MOSI:

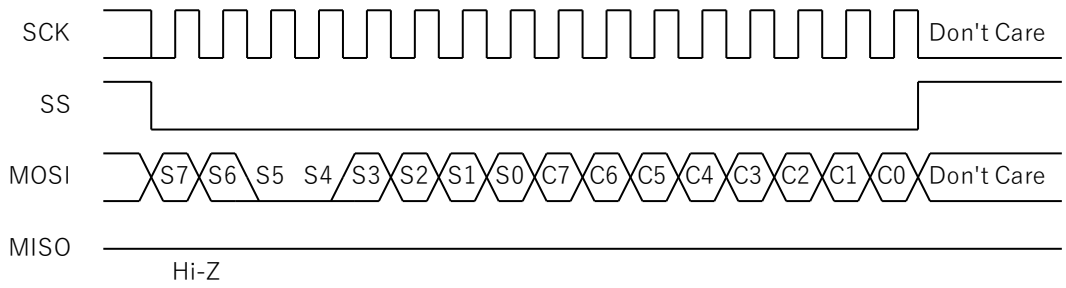
SEL	COM
S7 to S0	C7 to C0

SEL: Set “Device selection code” “Type selection code” and “Axis selection code”.
See “4.1.2.1.1 Axis selection (SEL)” for details.

COM: Set “Command code”.
See “4.3 Commands”.

4.1.2.2.1.2 Writing procedure

Write “Axis selection” and “Commands”.



S7 to S0: “Device selection code”, “Type selection code”, and “Axis selection code”.
(Since they are command writing format, "S5 = 0" and "S4 = 0")

C7 to C0: “Command code”

“Command code” should be wriltten at the rising of SS signal.

4.1.2.2.2. Writing registers

4.1.2.2.2.1 Axis selection, Command, Data (Register)

Write “Axis selection” and “Commands” by writing command format. “Data” is written as well.

	SEL	COM	DATx				DATy	DATz	DATu
MOSI:	S7 to S0	C7 to C0	D7 to D0	D15 to D8	D23 to D16	D31 to D24	Same as DATx	Same as DATx	Same as DATx

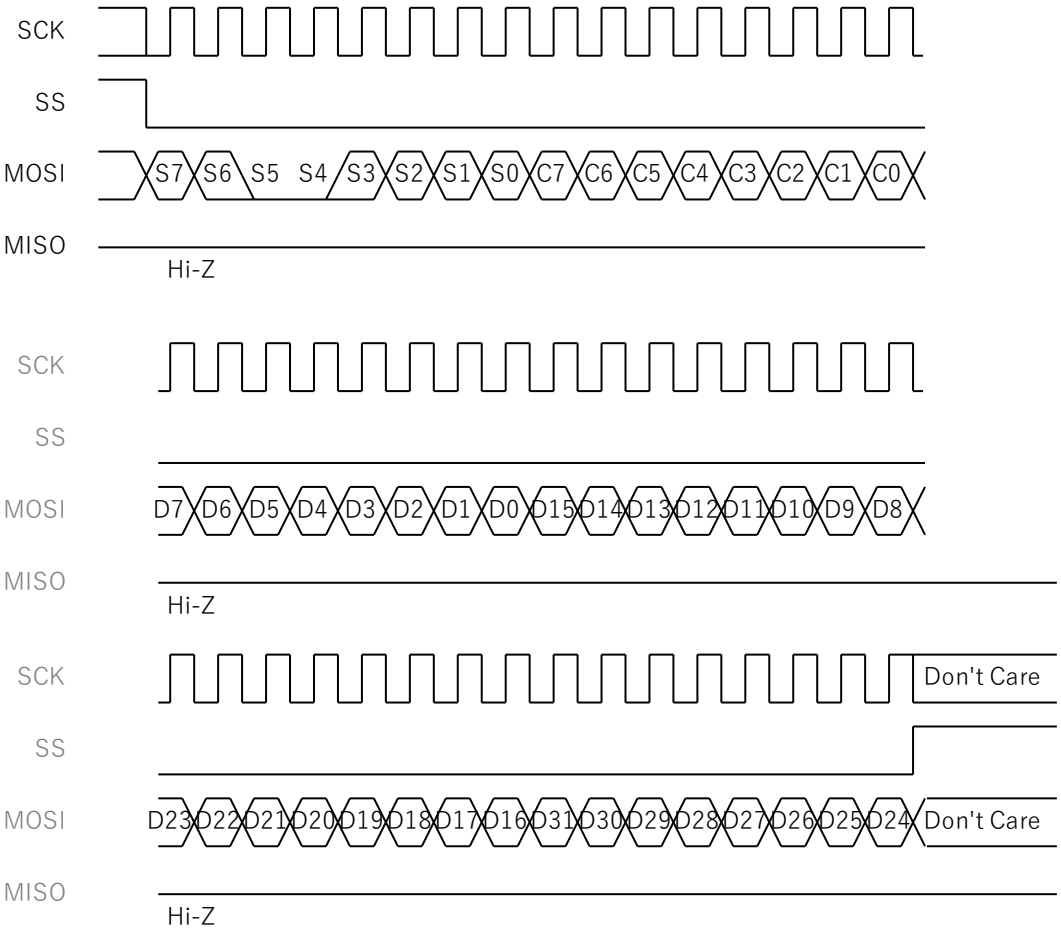
SEL: Set “Device selection code”, “Type selection code", and “Axis selection code”.
See “4.1.2.1.1 Axis selection (SEL)” for details.

COM: Set “Command code”.
See “4.3 Commands” for details.

DATx to DATu: Set “Data”.
See “4.1.2.1.3 Data (DAT)” for details.

4.1.2.2.2.2 Writing procedure

Write “Axis selection”, “Command” and “Data (register)”.



S7 to S0: “Device selection code” “Type selection code” “Axis selection code “
(Since they are command writing format, “S5 = 0” and “S4 = 0”.)

C7 to C0: “Command code”

D31 to D0: “Data” (For single-axis)

“Data” is written at the rising of SS signal.

4.1.2.2.3 Reading register

4.1.2.2.3.1 Axis selection, Commands, Data (Register)

Write “Axis selection” and “Command” by writing command format.

MOSI:

SEL	COM
S7 to S0	C7 to C0

Read “Data”.

MISO:

DATx				DATy	DATz	DATu
D7 to D0	D15 to D8	D23 to D16	D31 to D24	Same as DATx	Same as DATx	Same as DATx

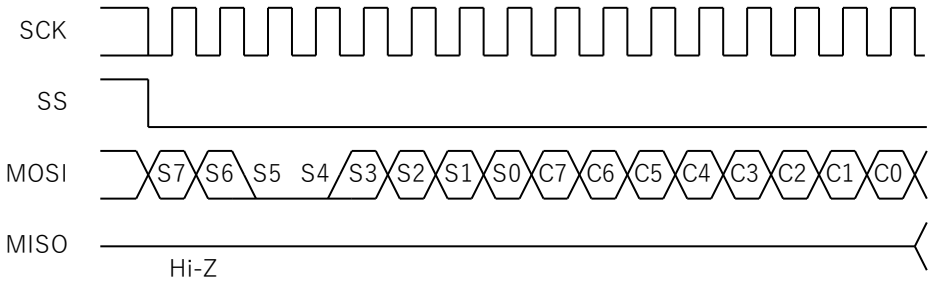
SEL: Set “Device selection code”, “Type selection code” and “Axis selection code”.
See “4.1.2.1.1 Axis selection (SEL) Axis selection (SEL)” for details.

COM: Set “Command code”.
See “4.3 Commands” for details.

DATx to DATu: Obtain “Data”.
See “4.1.2.1.3 Data (DAT)” for details.

4.1.2.2.3.2 Reading procedure

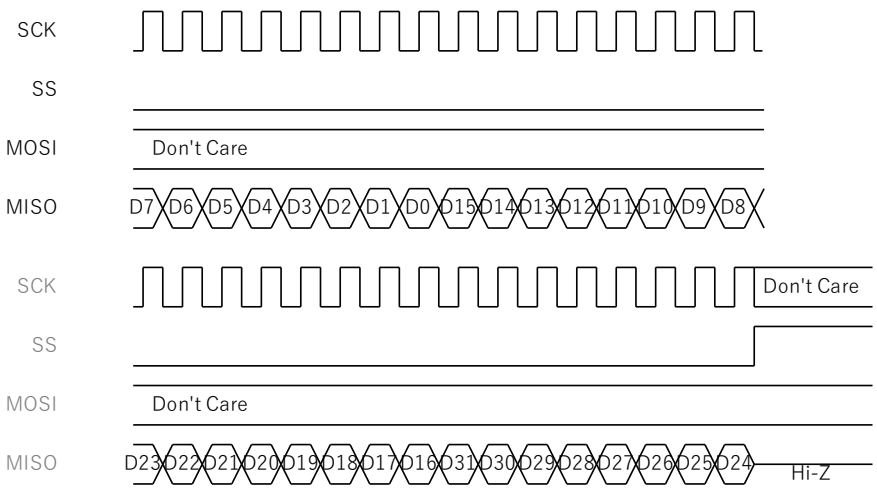
1) Write “Axis selection” and “Commands”.



S7 to S0: “Device selection code” “Type selection code” “Axis selection code”
(Since they are command write format, “S5 = 0” and “S4 = 0”.)

C7 to C0:“Command code”

2) Read “Data”.



D31 to D0:“Data” (For single-axis)

“Data” to be read latches the status at the time of writing “C0” bit of “Commands”.

4.1.2.2.4 Reading Main-status

4.1.2.2.4.1 Axis selection, Data (MSTS)

Write “Axis selection” by main-status reading format.

MOSI:

SEL
S7 to S0

Read “MSTS”.

MISO:

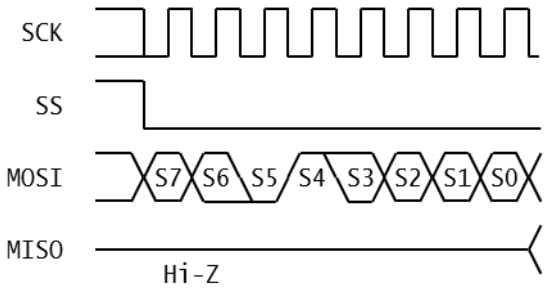
DATx		DATy	DATz	DATu
D7 to D0	D15 to D8	Same as DATx	Same as DATx	Same as DATx

SEL: Set “Device selection code”, “Type selection code” and “Axis selection code”.
See “4.1.2.1.1 Axis selection (SEL)” for details.

DATx to DATu: Obtain “MSTS”.
See “4.1.2.1.3 Data (DAT)” for details.

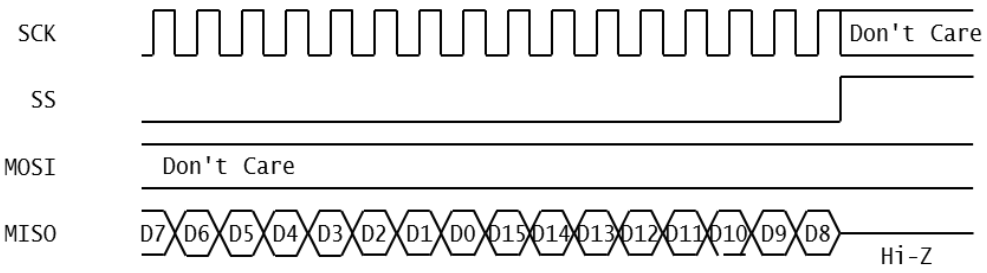
4.1.2.2.4.2 Reading procedure

1) Write “Axis selection”.



S7 to S0: “Device selection code” “Type selection code” “Axis selection code “
(Since they are main-status reading format, “S5 = 0” and “S4 = 0”.)

2) Read “MSTS”.



D15 to D0: “MSTS” (For single-axis)

“MSTS” to be read latches the status at the time of writing “S0” bit.

4.1.2.2.5 Writing general-purpose output port

4.1.2.2.5.1 Axis selection, Data (OTP)

Write “Axis selection” by general-purpose output port writing format, and write “OTP” as well.

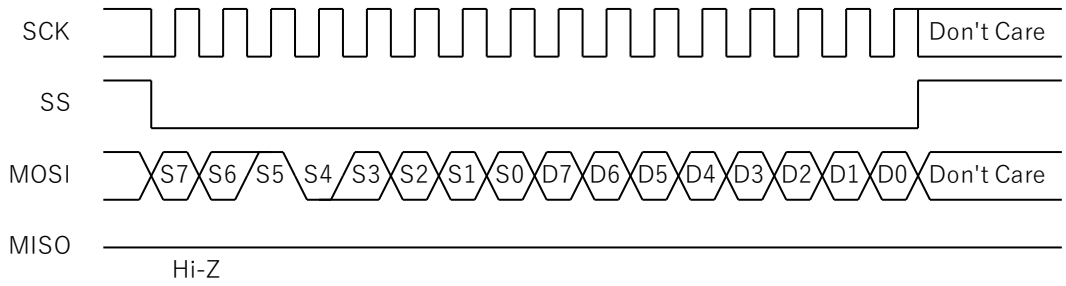
MOSI:	SEL	DATx	DATy	DATz	DATu
	S7 to S0	D7 to D0	Same as DATx	Same as DATx	Same as DATx

SEL: Set “Device selection code”, “Type selection code” and “Axis selection code”.
See “4.1.2.1.1 Axis selection (SEL)” for details.

DATx to DATu: Set “OTP”.
For “OTP”, see “4.2.2 Sub status (SSTS) and general-purpose I/O ports (IOP)” for details.

4.1.2.2.5.2 Writing procedure

Write “Axis selection” and “Data (OTP)”.



S7 to S0: “Device selection code” “Type selection code” “Axis selection code”
(Since they are general-purpose output port writing format, “S5 = 1” and “S4 = 0”.)

D7 to D0: “OTP” (For single-axis)

“OTP” is written at the rising of SS signal.

4.1.2.2.6 Read sub status and general-purpose I/O port

4.1.2.2.6.1 Axis selection, Data (SSTS, IOP)

Write “Axis selection” by sub status reading format.

MOSI:

SEL
S7 to S0

Read “SSTS” and “IOP”.

MISO:

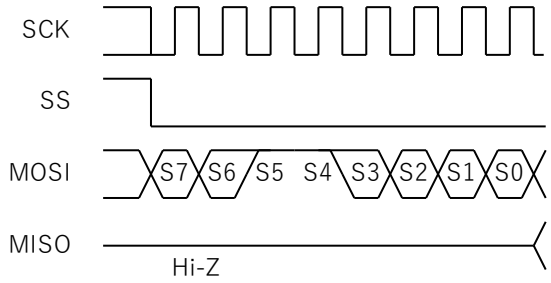
DATx		DATy	DATz	DATu
D7 to D0	D15 to D8	Same as DATx	Same as DATx	Same as DATx

SEL: Set “Device selection code”, “Type selection code” and “Axis selection code”.
See “4.1.2.1.1 Axis selection (SEL)” for details.

DATx to DATu: Obtain “SSTS” and “IOP”.
See “4.1.2.1.3 Data (DAT)” for details.

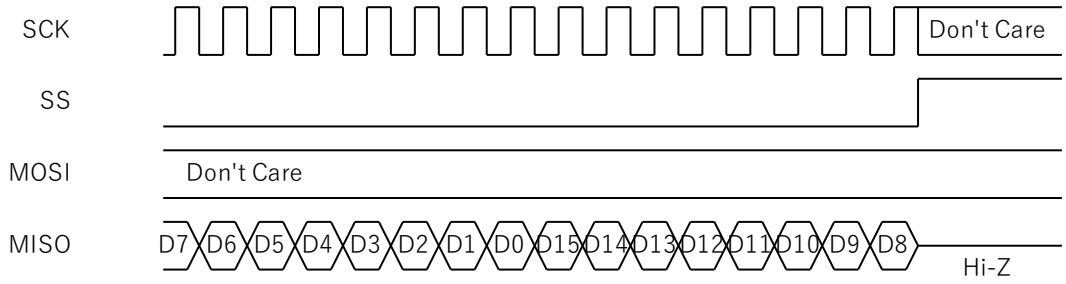
4.1.2.2.6.2 Read procedure

1) Write “Axis selection”.



S7 to S0:“Device selection code” “Type selection code” “Axis selection code”
(Since they are sub status reading format, “S5 = 1” and “S4 = 1”.)

2) Read “SSTS” and “IOP”.



D7 to D0: “IOP” (For single-axis)
D15 to D8: “SSTS” (For single-axis)

“SSTS” and “IOP” to be read latches the status at the time of writing “S0” bit.

4.2 Status

The status during parallel communication will be updated whenCLK signal is input once or more during “RD = H level”.

4.2.1 Main-status (MSTS)

Reads operation status, interrupt type, comparator and pre-register status.

MSTSW															
MSTSB1								MSTSB0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SPRF	SEOR	0	SCP4	SCP3	SCP2	SCP1	SSC1	SSC0	SINT	SERR	SEND	SENI	SRUN	SSCM

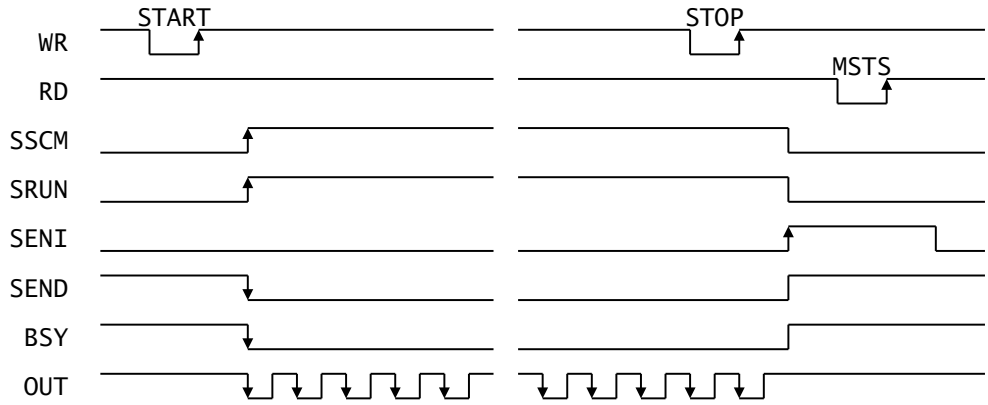
Bit	Name	Description
0	SSCM	0: No start command has been written after an operation has stopped or has been reset. 1: Start command has been written.
1	SRUN	0: “BSY = H level” (Stopping) 1: “BSY = L level” (Operating)
2	SENI	0: No stop interrupt occurred, or “RENV2.IEND = 0”. 1: Stop interrupt occurred. When “RENV2.MRST = 0”, it returns to “0” within 3 CLK signal cycles after reading. When “RENV2.MRST = 1”, it returns to “0” within 3 CLK signal cycles after writing SENIR (2Dh) command.
3	SEND	0: Start command is written or has never started after reset 1: Operation stopped
4	SERR	0: No error interrupt occurred. 1: Error interrupt occurred. When all bits in REST register become “0” from “1”, it returns to “0”.
5	SINT	0: No event interrupt occurred. 1: Event interrupt occurred. When all bits in RIST register become “0” from “1”, it returns to “0”.
7, 6	SSC	It is the sequence number (RMD.MSN) when operating or stopping. It can be used to check the step of operation blocks when creating the software.
8	SCP1	0: Comparator 1 condition is not met. 1: Comparator 1 condition is met.
9	SCP2	0: Comparator 2 condition is not met. 1: Comparator 2 condition is met.
10	SCP3	0: Value of target counter is equal to or less than RCMP 3 register value. 1: Value of target counter exceeds RCMP 3 register value. Comparison result monitor of comparator for software limit detection at positive side. The target counter is selected by software limit management counter selection (RENV3.SLCU). When not used, setting “RCMP3 = 7FFFFFFFh” (counter maximum value) can fix it to “MSTS.SCP3 = 0”.
11	SCP4	0: Value of target counter is equal to or more than RCMP 4 register value. 1: Value of target counter is less than RCMP 4 register value. Comparison result monitor of comparator for software limit detection at negative side. The target counter is selected by software limit management counter selection (RENV3.SLCU). When not used, setting “RCMP4 = 80000000h” (counter minimum value) can fix it to “MSTS.SCP4 = 0”.

Bit	Name	Description
12	Not defined	It is always “0”.

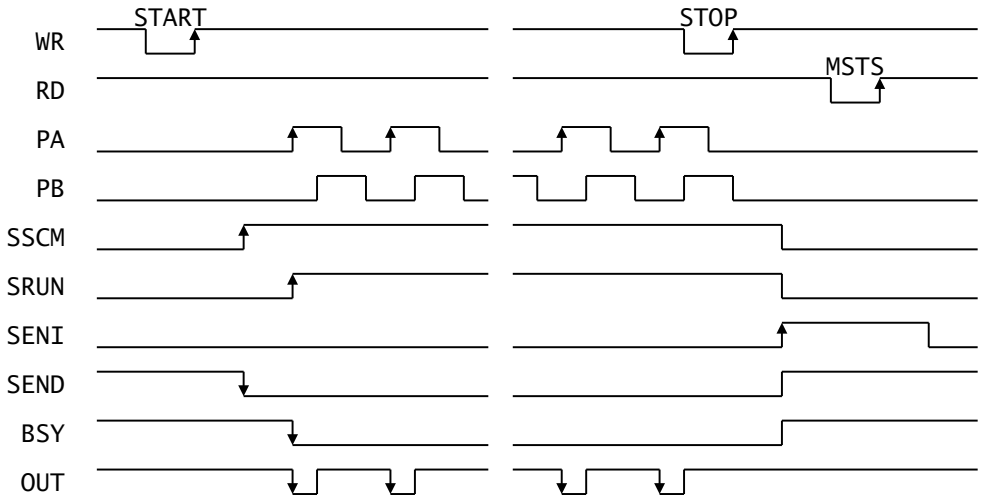
Bit	Name	Details
13	SEOR	0: Stopping at target position or operating. 1: Stopping at other than target position. It occurs when writing to the RMV register in the stopped state (the target position override has not been executed) and when RPLS > 0 (stopped without reaching the target position) in the stopped state. When “RENV2.MRST = 0”, it returns to “0” within 3 CLK signal cycles or less after reading. When “RENV2.MRST = 1”, it returns to “0” within 3 CLK signal cycles after writing SEORR (2Eh) command.
14	SPRF	0: Continuous operation data pre-register is “unfixed”. 1: Continuous operation data pre-register is “fixed”.
15	Not defined	It is always “0”.

The following are the examples of timings how the main-status changes when “RENV 2.IEND = 1” is set.

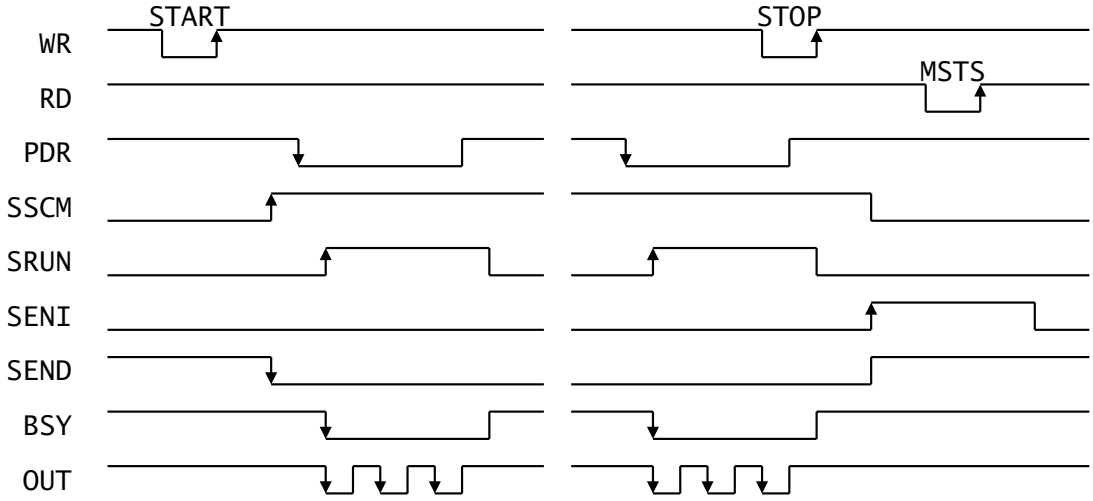
1. Command control continuous movement (RMD.MOD = 00h, 08h):



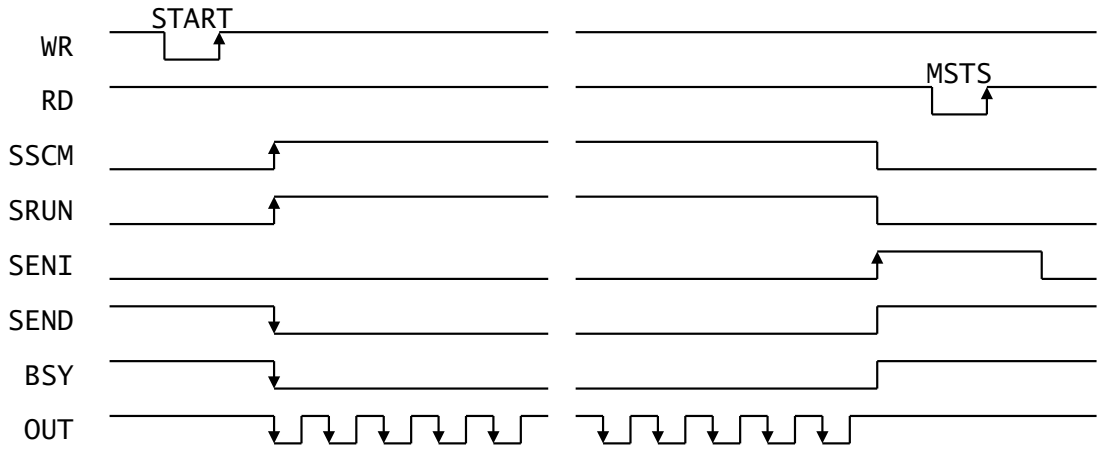
2. Pulser control continuous operations (RMD.MOD = 01h):



3. Continuous movement by switch control (RMD.MOD = 02h):



4. Stopped by positioning control such as incremental movement (RMD.MOD = 41h)



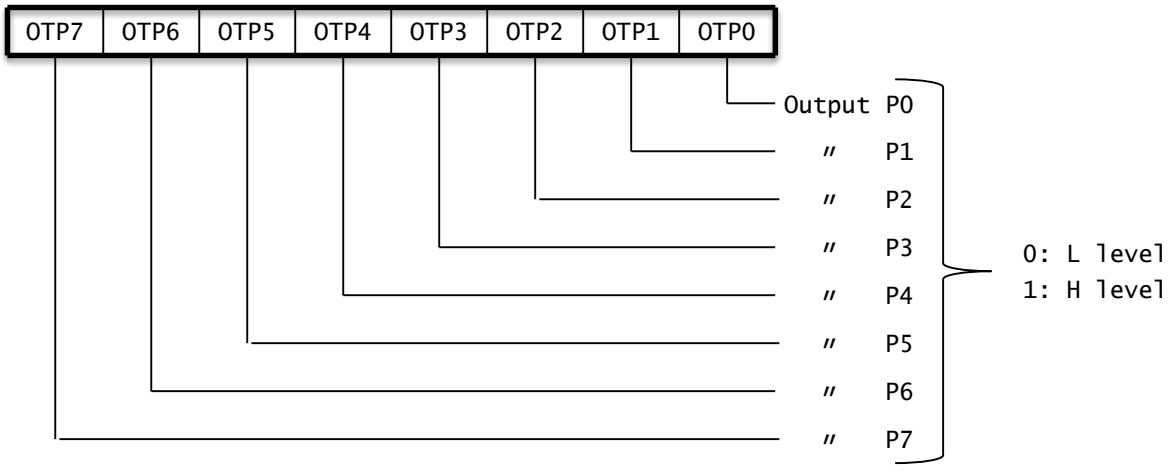
4.2.2 Sub status (SSTS) and general-purpose I/O ports (IOP)

Read the signal statuses of input terminals, the acceleration/deceleration statuses during operations and the signal statuses of general purpose I/O terminals.

SSTSW															
SSTSB								IOPB							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSD	SORG	SMEL	SPEL	SALM	SFC	SFD	SFU	IOP7	IOP6	IOP5	IOP4	IOP3	IOP2	IOP1	IOP0

Bit	Name	Description
7 to 0	IOP7 to 0	0: L level 1: H Level Read statuses of P7 to P0 terminals.
8	SFU	0: Other than accelerating 1: Accelerating.
9	SFD	0: Other than decelerating 1: Decelerating.
10	SFC	0: Other than constant speed operation 1: In constant speed operation
11	SALM	0: Alarm signal is OFF 1: Alarm signal is ON
12	SPEL	0: End limit signal at the positive side is OFF. 1: End limit signal at the positive side is ON.
13	SMEL	0: End limit signal at the negative side is OFF. 1: End limit signal at the negative side is ON.
14	SORG	0: Origin position signal is OFF. 1: Origin position signal is ON.
15	SSD	0: Signal to latch a slow-down signal is OFF. 1: Signal to latch a slow-down signal is ON. See “7.4.2 Slow-down signal (SDn)” for details.

Bit layout of general-purpose output port (OTP) is shown as follows:



4.2.3 Extension status (RSTS)

Read the signal status, operation status and operation direction of I/O terminals.

Extention status (RSTS) is in registers.

See “4.4.7.1 RSTS: Obtaining extension status register” for details.

4.3 Command

4.3.1 Operation commands

Start and stop the operation modes.

4.3.1.1 Start command

An operation starts if this command is written while stopped.

If written during an operation, it becomes the start command for the following operation.

COM	Name	Description
50h	STAFL	Start operations with the speed pattern of FL constant speed start.
51h	STAFH	Start operations with the speed pattern of FH constant speed start.
52h	STAD	Start operations with the speed pattern of high-speed start 1.
53h	STAUD	Start operations with the speed pattern of high-speed start 2.

For the details of speed patterns, see “6.1 Speed pattern list”.

4.3.1.2 Remaining pulse start command.

It can be used in the operation mode of positioning control incremental movement (RMD.MOD = 41h).

When writing after stopping on the way, it will operate for the number of remaining pulses in the positioning counter (RPLS).

Do not write this command during an operation.

COM	Name	Description
54h	CNTFL	Remaining pulses start with the FL constant start speed pattern.
55h	CNTFH	Remaining pulses start with the FH constant start speed pattern.
56h	CNTD	Remaining pulses start with the speed pattern of high- speed start 1.
57h	CNTUD	Remaining pulses start with the speed pattern of high-speed start 2.

4.3.1.3 Simultaneous start command

It start the axes waiting for simultaneous start signal input (RSTS.CND=0010b).

See “7.6 Simultaneous start” for details.

COM	Name	Description
06h	CMSTA	It outputs one-shot pulse in negative logic from CSTA terminal. It can be the input to CSTA terminal. If a simultaneous start signal input is being waited, the own-axis also starts.
2Ah	SPSTA	Simultaneous start signal is not output from CSTA terminal, and only the own-axis starts.

4.3.1.4 Speed change commands

It can be used in the operation mode of command control continuous movement (RMD.MOD = 00h, 08h) or positioning control incremental movement (RMD.MOD = 41h).

If these commands are written during operations, the axis changes its target speed and speed pattern.

Commands written while stopping are ignored.

COM	Name	Description
40h	FCHGL	Changes to FL speed immediately (change to the same operation pattern as the FL constant speed start).
41h	FCHGH	Changes to t FH speed immediately (change to the same operation pattern as the FH constant speed start).
42h	FSCHL	Decelerates to FL speed (change to the same operation pattern as high-speed start).
43h	FSCHH	Accelerates to FH speed (change to the same operation pattern as high-speed start).

4.3.1.5 Stop command

Writing this command will stop the axis.

COM	Name	Description
49h	STOP	Stops an axis immediately and exits the operation mode.
4Ah	SDSTP	Decelerates and stops and exits the operation mode.

4.3.1.6 Simultaneous stop command

Writing this command will stop an axis that is set to stop by simultaneous stop signal input (RMD.MSPE = 1). See “7.8 Simultaneous stop” for details.

COM	Name	Description
07h	CMSTP	Outputs one-shot pulse in negative logic from CSTP terminal. This signal can be an input to CSTP terminal. Own-axis is also stopped if the axis is set to stop by inputting a simultaneous stop signal.

4.3.1.7 Emergency stop command

COM	Name	Description
05h	CMEMG	Emergency stop all axes and exit the operation mode.

4.3.2 General-purpose output bit control commands

Controls P0 to P7 terminals that are set as general-purpose output terminals per 1 bit.

The command for the terminal corresponding to general-purpose input terminal is ignored.

When controlling all 8-bit at a time, write to general output port.

See "4.1.1.2.5 Write to general-purpose output port" or "4.1.2.2.5 Writing general-purpose output port" for details.

4.3.2.1 Output reset command

Resets the corresponding general-purpose output terminal to L level.

COM	Name	Description
10h	P0RST	Reset P0 terminal that has been set as a general-purpose output terminal to L level.
11h	P1RST	Reset P1 terminal that has been set as a general-purpose output terminal to L level.
12h	P2RST	Reset P2 terminal that has been set as a general-purpose output terminal to L level.
13h	P3RST	Reset P3 terminal that has been set as a general-purpose output terminal to L level.
14h	P4RST	Reset P4 terminal that has been set as a general-purpose output terminal to L level.
15h	P5RST	Reset P5 terminal that has been set as a general-purpose output terminal to L level.
16h	P6RST	Reset P6 terminal that has been set as a general-purpose output terminal to L level.
17h	P7RST	Reset P7 terminal that has been set as a general-purpose output terminal to L level.

4.3.2.2 Output set command

Sets the corresponding general-purpose output terminal to H level

COM	Name	Description
18h	P0SET	Set P0 terminal that has been set as a general-purpose output terminal to H level.
19h	P1SET	Set P1 terminal that has been set as a general-purpose output terminal to H level.
1Ah	P2SET	Set P2 terminal that has been set as a general-purpose output terminal to H level.
1Bh	P3SET	Set P3 terminal that has been set as a general-purpose output terminal to H level.
1Ch	P4SET	Set P4 terminal that has been set as a general-purpose output terminal to H level.
1Dh	P5SET	Set P5 terminal that has been set as a general-purpose output terminal to H level.
1Eh	P6SET	Set P6 terminal that has been set as a general-purpose output terminal to H level.
1Fh	P7SET	Set P7 terminal that has been set as a general-purpose output terminal to H level.

4.3.3 Control commands

4.3.3.1 Software reset command

COM	Name	Description
04h	SRST	Resets LSI with software. After writing this command, wait for access for 12 cycles of CLK signal (0.6 µs).

4.3.3.2 Counter clear command

Sets “0” in the counter.

COM	Name	Description
20h	CUN1R	Clear COUNTER 1 (RCUN1).
21h	CUN2R	Clear COUNTER 2 (RCUN2).

4.3.3.3 ERC output control command

Controls the output of deviation counter clear signals.

COM	Name	Description
24h	ERCOUT	Outputs the deviation counter clear signal from ERCn terminal.
25h	ERCRST	Resets the output from ERCn terminal.

4.3.3.4 Pre-register control command

COM	Name	Description
26h	PRECAN	Cancels the pre-register confirmation status. See “4.4.1 Pre-register” for details.

4.3.3.5 Target position override 2 start command

COMB0	Name	Description
28h	STAON	Start positioning control of target position override 2.

4.3.3.6 Latch control command

Controls latches of counters.

COM	Name	Description
29h	LTCH	Latch RCUN1 register value to RLTC1 register and RCUN2 register value to RLTC2 register.
3Ch	LTC3E	Start monitoring of the trigger signal for RLTC3 register latch.
3Dh	LTC4E	Start monitoring of the trigger signal for RLTC4 register latch.
3Eh	LTC3D	Terminate monitoring the trigger signal for RLTC3 register latch.
3Fh	LTC4D	Terminate monitoring the trigger signal for RLTC4 register latch.

4.3.3.7 SENI, SEOR clear command

This command clears each bit of the main-status (MSTS) manually.

It is used when “RENV2.MRST = 1” (write manual clear).

COM	Name	Description
2Dh	SENIR	Clear stop interrupt bit (MSTSW.SENI).
2Eh	SEORR	Clear bit that shows stop other than target position (MSTS.SEOR).

4.3.3.8 ID code confirmation command

COM	Name	Description
03h	IDMON	Sets ID code in the upper 16 bits of RMG register. The set ID code can be read only once with RRMG (D5h) command. Cleared by writing commands other than IDMON (03h) command. See “7.14 ID Monitor” for details.

4.3.3.9 NOP (disabled) command

COM	Name	Description
00h	NOP	It does not affect operations. Writing commands will be processed.

4.3.4 Register control commands

Data will be copied between register and I/O buffer by writing register control command.

4.3.4.1 Register control command list

The following registers are dedicated for each axis. You can access individual dedicated registers from each axis

No.	Contents	Length	Register					Pre-register				
			Name	Read command		Write command		Name	Read command		Write command	
				COMB0	Name	COMB0	Name		COMB0	Name	COMB0	Name
1	Feeding amount setting	32	RMV	D0h	RRMV	90h	WRMV	PRMV	C0h	RPRMV	80h	WPRMV
2	FL speed setting	14	RFL	D1h	RRFL	91h	WRFL	PRFL	C1h	RPRFL	81h	WPRFL
3	FH speed setting	14	RFH	D2h	RRFH	92h	WRFH	PRFH	C2h	RPRFH	82h	WPRFH
4	Acceleration rate	16	RUR	D3h	RRUR	93h	WRUR	PRUR	C3h	RPRUR	83h	WPRUR
5	Deceleration rate	16	RDR	D4h	RRDR	94h	WRDR	PRDR	C4h	RPRDR	84h	WPRDR
6	Speed magnification rate setting, ID code obtaining	32	RMG	D5h	RRMG	95h	WRMG	PRMG	C5h	RPRMG	85h	WPRMG
7	Slow-down point setting	24	RDP	D6h	RRDP	96h	WRDP	PRDP	C6h	RPRDP	86h	WPRDP
8	Operation mode setting	30	RMD	D7h	RRMD	97h	WRMD	PRMD	C7h	RPRMD	87h	WPRMD
9	Linear interpolation main axis feeding amount setting	32	RIP	D8h	RRIP	98h	WRIP	PRIP	C8h	RPRIP	88h	WPRIP
10	Acceleration S-curve section setting	13	RUS	D9h	RRUS	99h	WRUS	PRUS	C9h	RPRUS	89h	WPRUS
11	Deceleration S-curve section setting	13	RDS	DAh	RRDS	9Ah	WRDS	PRDS	CAh	RPRDS	8Ah	WPRDS
12	Environment setting 1	32	RENV1	DCh	RRENV1	9Ch	WRENV1	-	-	-	-	-
13	Environment setting 2	32	RENV2	DDh	RRENV2	9Dh	WRENV2	-	-	-	-	-
14	Environment setting 3	26	RENV3	DEh	RRENV3	9Eh	WRENV3	-	-	-	-	-
15	Environment setting 4	16	RENV4	DFh	RRENV4	9Fh	WRENV4					
16	COUNTER 1	32	RCUN1	E3h	RRCUN1	A3h	WRCUN1	-	-	-	-	-
17	COUNTER 2	32	RCUN2	E4h	RRCUN2	A4h	WRCUN2	-	-	-	-	-
18	Comparison data 1	32	RCMP1	E7h	RRCMP1	A7h	WRCMP1	-	-	-	-	-
19	Comparison data 2	32	RCMP2	E8h	RRCMP2	A8h	WRCMP2	-	-	-	-	-
20	Comparison data 3	32	RCMP3	E9h	RRCMP3	A9h	WRCMP3	-	-	-	-	-
21	Comparison data 4	32	RCMP4	EAh	RRCMP4	AAh	WRCMP4	-	-	-	-	-
22	Event interrupt factor setting	18	RIRQ	ECh	RRIRQ	ACh	WRIRQ	-	-	-	-	-
23	Latch data 1	32	RLTC1	EDh	RRLTC1	-	-	-	-	-	-	-
24	Latch data 2	32	RLTC2	EEh	RRLTC2	-	-	-	-	-	-	-
25	Latch data 3	32	RLTC3	EFh	RRLTC3	-	-	-	-	-	-	-
26	Latch data 4	32	RLTC4	F0h	RRLTC4							
27	Extension status obtaining	23	RSTS	F1h	RRSTS							
28	Error interrupt factor obtaining	11	REST	F2h	RREST	B2h	WREST					
29	Event interrupt factor obtaining	20	RIST	F3h	RRIST	B3h	WRIST					
30	Positioning counter obtaining	32	RPLS	F4h	RRPLS							
31	Current position, EZ counts obtaining	20	RSPD	F5h	RRSPD	-	-	-	-	-	-	-
32	Slow-down points obtaining	24	RSDC	F6h	RRSDC	-	-	-	-	-	-	-

The following are the shared registers for all axes. You can access the identical shared registers from all axes.

No.	Contents	Length	Register					Pre-register				
			Name	Read command		Write command		Name	Read command		Write command	
				COMB0	Name	COMB0	Name		COMB0	Name	COMB0	Name
1	Common I/ port (GP0 to GP15) management	16	RGPM	FAh	RRGPM	BAh	WRGPM	-	-	-	-	-
2	Common I/O port (GP0 to GP15) information	16	RGPD	FBh	RRGPD	BBh	WRGPD	-	-	-	-	-

For details on register contents, see “4.4 Registers (Pre-registers)”.

4.4 Register (Pre-registers)

All registers (pre-registers) go to “0” after resetting, but “0” can be out of the setting range in some registers. The negative number representation of signed numbers is two’s complement.

Except for start commands, no re-writing is required when the value to be set is the same as the last time.

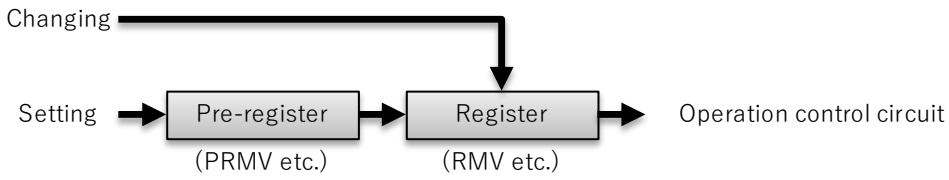
Several registers (pre-registers) can be written and all registers (pre-registers) can be read.

Note:

1. Bits marked with “*” will ignore writing and reading will be “0”.
2. Bits marked with “&” will ignore writing and reading will be the same as the most significant bit in the blank display (sign extension).

4.4.1 Pre-register

RMV, RFL, RFH, RUR, RDR, RMG, RDP, RMD, RIP, RUS, RDS registers and start commands have the pre-registers. The pre-register is a register to set the continuous operation data and the continuous operation start command during the current operation. It is configured as shown below; it operates with FIFO.



4.4.1.1 Writing to pre-register

There are 2 stages; a pre-register and a register. Up to two operation data can be held.

If the register has a pre-register, data should be written to the pre-register.

No need to rewrite the pre-registers of registers that have not changed.

Data that was written to the pre-register during stopping will shift to the register and will become the register data.

The data written to the pre-register during operation becomes the pre-register data.

Register data and pre-register data are fixed by writing a start command (STAFL, STAFH, STAD, and STAUD).

When the current operation is completed, the fixed data in pre-register will shift to the register and the axis will automatically start.

The status of pre-register can be checked by MSTS.SPRF bit.

Data cannot be written to pre-registers if “MSTS.SPRF = 1”.

When changing the target position or the target speed (overriding) during an operation, write new data to the registers.

The following shows the relationship between writing status of pre-register and MSTS.SPRF bit:

No	Procedure	Pre-register	Register	SPRF
1.	Initial status while stopping.	0 (Unfixed)	0 (Fixed)	0
2.	While stopping, write data 1 to pre-register. Data 1 is automatically copied to register.	Data 1 (Unfixed)	Data 1 (Unfixed)	0
3.	Write start command. Data 1 in register is fixed and start operation of data 1.	Data 1 (Unfixed)	Data 1 (Fixed)	0
4.	Write data 2 to pre-register for a continuous operation during the operation of data 1. Writing can be skipped in pre-register if the data is the same as the previous one. Since the data is fixed, data 2 will not be automatically copied to register.	Data 2 (Unfixed)	Data 1 (Fixed)	0
5.	Write start command for the continuous operation Data 2 in the pre-register is fixed, and the completion of the operation of data 1 is awaited. Since data 2 in the pre-register is fixed, data 3 cannot be written even if it exists.	Data 2 (Fixed)	Data 1 (Fixed)	1
6.	Operation of data 1 is completed. Data 2 is automatically copied to register, and continuously operates. Since pre-register becomes “Unfixed”, data 3 can be written.	Data 2 (Unfixed)	Data 2 (Unfixed)	0
7.	Operation of data 2 is completed. Since register becomes “Unfixed, the operation will stop.	Data 2 (Unfixed)	Data 2 (Unfixed)	0

If an event interrupt occurs when pre-register is enabled to write (RIRQ.IRNM) is set, an event interrupt (RIST.ISNM) can be generated when the pre-register changes to “Unfixed”.

Note: When continuous operation is automatically started using a pre-register, set the operation completion timing to “PRMD.METM = 0” (output pulse cycle completion).

When “PRMD.METM = 1” (output pulse ON width complete) is set, the interval between the last pulse and the first pulse of continuous operation is narrowed to 16 ×T_{CLK} (T_{CLK}: reference clock cycle).

See “7.3.2 Output pulse width and operation complete timing” for details.

4.4.1.2 Cancel pre-register data

Pre-register data is canceled in the following cases.

1. Write PRECAN (26h) command.
   →You can change pre-register data and start commands by changing pre-register to “Unfixed” from “Fixed”.
2. Stop by writing STOP (49h) command or SDSTP (4Ah) command.
   →Writing SDSTP (4Ah) command during automatic deceleration in incremental movement operation mode will cancel it after reaching the target position.
3. Stop due to error interrupt occurrence factor.

4.4.2 Speed control registers

The following are the registers for speed control.

No.	Name	Description	Bit length	Range			R/W
1	RFL (PRFL)	FL speed setting	14	1	to	16,383 (3FFFh)	R/W
2	RFH (PRFH)	FH speed setting	14	1	to	16,383 (3FFFh)	R/W
3	RUR (PRUR)	Acceleration rate setting	16	1	to	65,535 (FFFFh)	R/W
4	RDR (PRDR)	Deceleration rate setting	16	0	to	65,535 (FFFFh)	R/W
5	RMG (PRMG)	Speed magnification rate setting	12	1	to	4,095 (FFFh)	R/W
		Obtain ID code	16		-		
6	RDP (PRDP)	Slow-down point setting	24	-8,388,608 (800000h)	to	+8,388,607 (7FFFFFh)	R/W
				0	to	16,777,215 (FFFFFFh)	R/W
7	RUS (PRUS)	S-curve section during acceleration setting	13	0	to	8,191 (1FFFh)	R/W
8	RDS (PRDS)	S-curve section during deceleration setting	13	0	to	8,191 (1FFFh)	R/W
9	RSPD	Obtain current speed	14	0	to	16,383 (3FFFh)	R
		Obtain EZ count	4	0	to	15 (Fh)	
10	RSDC	Obtain slow-down point	24	-8,388,608 (800000h)	to	+8,388,607 (7FFFFFh)	R
				0	to	16,777,215 (FFFFFFh)	

Note: “0” is out of the setting range of registers and pre-registers in; RFL (PRFL), RFH (PRFH), RUR (PRUR), and RMG (PRMG).

4.4.2.1 RFL (PRFL): FL speed setting register

It is used to set FL speed (initial speed/stop speed) for high-speed start (acceleration/deceleration operations). PRFL is the pre-register for RFL register.

[WPRFL: 81h, RPRFL: C1h]
[WRFL: 91h, RRFL: D1h]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*														

Setting range: 1 to 16,383 (3FFFh)

The actual FL speed [pps] is calculated with the value in RMG register.

See “6.2 Speed pattern settings” for details.

4.4.2.2 RFH (PRFH): FH speed setting register

It is used to set FH speed (operation speed).
PRFH is the pre-register for RFH register.
During operation, RFH register can be changed to override the target speed.

[WPRFH: 82h, RPRFH: C2h]
[WRFH: 92h, RRFH: D2h]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*														

Setting range is 1 to 16,383(3FFFh)

The actual FH speed [pps] is calculated with the value in RMG register.

See “6.2 Speed pattern settings” for details.

4.4.2.3 RUR (PRUR): Acceleration rate setting register

It is used to set acceleration rate.
PRUR is the pre-register for RUR register.

[WPRUR: 83h, RPRUR: C3h]
[WRUR: 93h, RRUR: D3h]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*																

Setting range: 1 to 65,535(FFFFh)

See “6.2 Speed pattern settings” for details.

4.4.2.4 DR (PRDR): Deceleration rate setting register

It is used to set deceleration rate.
PRDR is the pre-register for RDR register.

[WPRDR: 84h, RPRDR: C4h]
[WRDR: 94h, RRDR: D4h]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*																

Setting range: 1 to 65,535 (FFFFh)

When RDR = “0”, deceleration rate will be the value set in RUR register

See “6.2 Speed pattern settings”.

Note: When automatic setting is selected for slow-down point (“RMD.MSDP = 0”), enter the same value as used in RUR register or “0”.

4.4.2.5 RMG (PRMG): Speed magnification rate setting register

It is used to set speed magnification rate. [WPRMG: 85h, RPRMG: C5h]
PRMG is the pre-register for RMG register. [WRMG: 95h, RRMG: D5h]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	MG											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IDCD															

Position	Name	Description
11 to 0	MG	Setting range is 1 to 4,095. Set the relationship between set values in RFL or RFH registers and the actual speeds. The actual speeds [pps] are products of speed magnification rate and the value set in speed register. See “6.2 Speed pattern settings” for details.
15 to 12	(Undefined)	Always set “0”.
31 to 16	IDCD	IDCD bit exists only in RMG register. ID code can be read only immediately after IDMON (03h) command is written. Usually “0” is read. Writing this bit is ignored. See “7.14 ID Monitor” for details.

[Example to set magnification rate when reference clock frequency = 19.6608 MHz]

Setting value	Magnification rate	Actual speed range [pps]	Setting value	Magnification rate	Actual speed range [pps]
3999 (0F9Fh)	0.3	0.3 to 4,914.9	59 (003Bh)	20	20 to 327,660
2399 (095Fh)	0.5	0.5 to 8,191.5	23 (0017h)	50	50 to 819,150
1199 (04AFh)	1	1 to 16,383	11 (000Bh)	100	100 to 1,638,300
599 (0257h)	2	2 to 32,766	5 (0005h)	200	200 to 3,276,600
239 (00EFh)	5	5 to 81,915	2 (0002h)	400	400 to 6,553,200
119 (0077h)	10	10 to 163,830	1 (0001h)	600	600 to 9,829,800

4.4.2.6 RDP (PRDP): Slow-down point setting register.

This register sets the slow-down point to be used in incremental movement operation mode. [WPRDP: 86h, RPRDP: C6h]
PRDP is the pre-register for RDP register. [WRDP: 96h, RRDP: D6h]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
#	#	#	#	#	#	#	#																								

Bits marked with name "#" are ignored when they are written. When they are read, the contents vary according to the slow-down point setting (RMD.MSDP).

MSDP	Setting details	bit #
0	Setting range is -8,388,608 to +8,388,607. It is an offset to the automatic setting value of slow-down point. When a positive number is entered, deceleration starts earlier, and FL speed section will be longer. When a negative number is entered, deceleration starts later, and the speed will not reach FL speed.	Same as bit 23.
1	Setting range is 0 to 16,777,215. It is a manual setting value for slow-down point. Deceleration will start when the remaining feeding amount becomes less than the set value.	0

See "6.2 Speed pattern settings" for details.

4.4.2.7 RUS (PRUS): Acceleration S-curve section setting register

It is used to specify S-curve section in S-curve acceleration. [WPRUS: 89h, RPRUS: C9h]
PRUS is the pre-register for RUS register. [WRUS: 99h, RRUS: D9h]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*													

Setting range is 0 to 8,191

When "0" is entered, it will create a complete S-curve acceleration with no linear section by substituting $\frac{RFH-RFL}{2}$.

4.4.2.8 RDS (PRDS): Deceleration S-curve section setting register

It is used to specify S-curve section in S-curve deceleration. [WPRDS: 8Ah, RPRDS: CAh]
PRDS is the pre-register for RDS register. [WRDS: 9Ah, RRDS: DAh]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*													

Setting range is 0 to 8,191

When "0" is entered, it will create a complete S-curve deceleration with no linear section by substituting $\frac{RFH-RFL}{2}$.

Note: Specify the same value as in PRUS register if slow-down point setting is "RMD.MSDP = 0" (automatic setting).

4.4.2.9 RSPD: Current speed obtaining register

It is used to obtain current speed and EZ count value. [RRSPD: F5h]
(Read only.)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	AS													

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	EZC			

Position	Name	Description
13 to 0	AS	Current speed can be read as a step value (the same units as in RFL or RFH register). It is “0” when stopping. It becomes a step value for the set speed (RFH register value) during a pulser control.
15 to 14	(Undefined)	(It is always “0”.)
19 to 16	EZC	Read the input count value of encoder Z-phase signal used for an origin return control. It is a down counter; it becomes the value of RENV2.EZD bit while stopping. See “5.5 Origin return control” for details.
31 to 20	(Undefined)	(It is always “0”.)

4.4.2.10 RSDC: Slow-down point obtaining register

It is used to acquire the slow-down point in an incremental movement operation mode. [RRSDC: F6h]
(Read only.)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
&	&	&	&	&	&	&	&																								

Slow-down point will change by the slow-down point setting method (RMD.MSDP).

MSDP	Description
0	The sum of automatically calculated “slow-down point automatic setting value” and “value in RDP” is shown in 24 bits Since “automatic slow-down point” is automatically calculated, it will be updated during acceleration/deceleration
1	The value is equal to the value in RDP register.

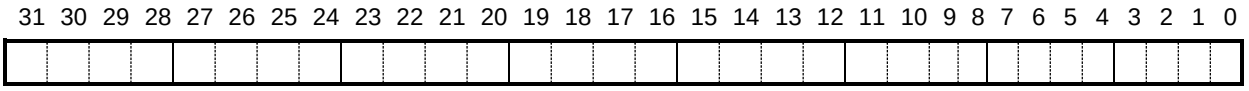
4.4.3 Position control register

The following are the registers for position control operations:

No.	Name	Description	Bit length	Range	R/W
1.	RMV (PRMV)	Sets feeding amount (=target position)	32	-2,147,483,648 (80000000h) to +2,147,483,647 (7FFFFFFFh)	R/W
2.	RIP (PRIP)	Sets feeding amount of the main axis for linear interpolation	32	0 to 2,147,483,648 (80000000h)	R/W
3.	RPLS	Acquiring positioning counter (Obtain remaining pulse feeding amount)	32	0 to 2,147,483,648 (80000000h)	R

4.4.3.1 RMV (PRMV): Feeding amount (target position) setting register

Register to set feeding amount (target postion) in incremental movement operation mode. [WPRMV: 80h, RPRMV: C0h]
PRMV is the pre-register for RMV register. [WRMV: 90h, RRMV: D0h]

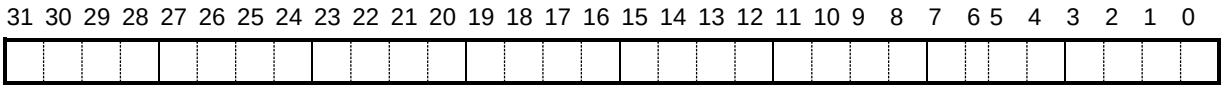


Setting range is –2,147,483,648 to +2,147,483,647.

The target position can be changed by re-writing RMV register while in positioning control of incremental movement operation mode (RMD.MOD=41h). See “7.2.1 Target position override 1 (RMV register)” for details.

4.4.3.2 RIP (PRIP): Main axis feeding amount in linear interpolation setting register

Register to set the absolute value of RMV register of an interpolated axis with the largest feeding amount in linear interpolation operations. PRIP is the pre-register for RIP register. [WPRIP: 88h, RPRIP: C8h] [WRIP: 98h, RRIP: D8h]



Setting range is 0 to 2,147,483,648

RIP register is used when RMD.MOD is as follows:

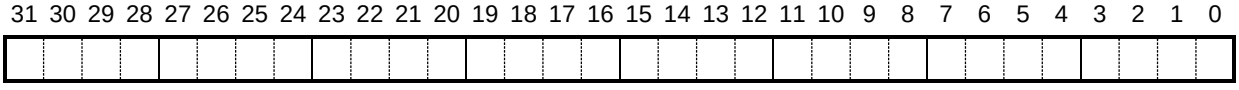
110 0010b (62h): Continuous movement operation mode in linear interpolation

110 0011b (63h): Incremental movement operation mode in linear interpolation

See “5.6 Linear interpolation control” for details.

4.4.3.3 RPLS: Positioning counter acquiring register

Register to acquire the remaining pulse feeding amount in incremental movement operation mode (Read only.) [RRPLS: F4h]



Value range is 0 to 2,147,483,648.

It becomes “0” when writing to RMV register.

When it starts, the value in RMV register is copied and it counts down at every pulse output.

4.4.4 Environment setting registers

The followings are registers for environment setting:

No.	Name	Description	Length	Range	R/W
1.	RMD (PRMD)	Operation mode setting	30	-	R/W
2.	RENV1	Environment setting 1	32	-	R/W
3.	RENV2	Environment setting 2	32	-	R/W
4.	RENV3	Environment setting 3	26	-	R/W
5.	RENV4	Environment setting 4	16	-	R/W
6.	RGPM	Shared I/O port management	16	-	R/W
7.	RGPD	Shared I/O port information	16	-	R/W

4.4.4.1 RMD (PRMD): Operation mode setting register

Register to set operation modes. [WPRMD: 87h, RPRMD: C7h]
PRMD is the pre-register for RMD register. [WRMD: 97h, RRMD: D7h]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	MPCS	MSDP	METM	MCCE	MSMD	MINP	MSDE	0	MOD						

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	MCDO	MCDE	0	MADJ	MSPO	MSPE	MAX3	MAX2	MAX1	MAX0	MSY		MSN	

Position	Name	Description
6 to 0	MOD	Sets operation modes: 000 0000b (00h): Positive direction continuous movement operation mode by command control. 000 1000b (08h): Negative direction continuous movement operation mode by command control. 000 0001b (01h): Continuous movement operation mode controlled by pulser control. 000 0010b (02h): Continuous movement operation mode by switch control. 001 0000b (10h): Positive direction origin return operation mode by origin return control. 001 1000b (18h): Negative direction origin return operation mode by origin return control. 100 0001b (41h): Incremental movement operation mode by positioning control. 100 0111b (47h): Timer operation mode by positioning control. 101 0001b (51h): Incremental movement operation mode by pulser control. 101 0110b (56h): Incremental movement operation mode by switch control. 110 0010b (62h): Continuous movement operation mode by linear interpolation control. 110 0011b (63h): Incremental movement operation mode by linear interpolation control.
7	(Undefined)	Always set “0”.
8	MSDE	Selects input functions of SDn terminal. 0: General-purpose input. SDn terminal status can be obtained by RSTS.SDIN bit. 1: Decelerates or deceleration stop can be done by turning slow-down signal ON.

<table>
<tr><th>Position</th><th>Name</th><th>Description</th></tr>
<tr><td>9</td><td>MINP</td><td>Selects input functions of INPn terminal.
0: General-purpose input.
INPn terminal status can be obtained by RSTS.SINP bit.
1: Operation completion is delayed until in-position signal turns ON.</td></tr>
<tr><td>10</td><td>MSMD</td><td>Selects acceleration/deceleration operations.
0: Linear acceleration/deceleration.
1: S-curve acceleration/deceleration.</td></tr>
<tr><td>11</td><td>MCCE</td><td>Selects count functions for command pulses.
0: Count command pulses.
1: Not count command pulses. Count encoder signals.</td></tr>
<tr><td>12</td><td>METM</td><td>Selects operation complete timing.
Operation complete timing can be advanced.
0: Select output pulse cycle completion.
1: Select output pulse ON width completion.</td></tr>
<tr><td>13</td><td>MSDP</td><td>Selects slow-down point setting method.
Slow-down point can be set manually.
0: Automatic setting:
It is conditional that:
“RUR = RDR”, “RUS = RDS” and “Result of automatic setting is signed 24 bits or less”.
1: Select “manual setting”.</td></tr>
<tr><td>14</td><td>MPCS</td><td>Selects input functions for PCSn terminals.
0: General-purpose input
When “RENV1.PCSM = 1”, it becomes the input terminal of the own-axis start signal.
1: Wait for pulse count start signal input at target position override 2.
Until pulse count start signal is input, it operates like the continuous movement operation mode.
When “RENV1.PCSM = 1”, it becomes the input terminal of the own-axis start signal.
<table>
<tr><th>RMD.MPCS</th><th>RENV1.PCSM</th><th>PCSn terminals</th></tr>
<tr><td>0</td><td>0</td><td>General-purpose input</td></tr>
<tr><td>0</td><td>1</td><td>Start own-axis</td></tr>
<tr><td>1</td><td>0</td><td>Start pulse count</td></tr>
<tr><td>1</td><td>1</td><td>Start own-axis</td></tr>
</table>
For details, see “7.2.2 Target position override 2 (PCSn)”.</td></tr>
<tr><td>15</td><td>(Undefined)</td><td>Always set to “0”.</td></tr>
</table>

Position	Name	Description
17,16	MSN	Sets 2-bit sequence number. The sequence number can be acquired with the MSTS.SSC bit, and it does not affect operations. When creating control software, it can be used for step management of operation blocks.
19, 18	MSY	Selects the start timing after writing a start command. 00b: Start immediately. 01b: Start with SPSTA (2Ah) command. If “RENV1.PCSM = 0”, also start when “CSTA = L level”. If “RENV1.PCSM = 1”, also start when “PCSn terminal turns ON. 10b: Start by internal synchronous signal (RENV3.SYI). See “7.12.2 Start by internal synchronous signal” for details. 11b: Start by stop of target axis (RMD.MAX0 to 3) See “7.12.1 Starts by stopping the target axis” for details.
20	MAX0	Selects whether to include X-axis in the target axis when “RMD.MSY = 11b”. 0: Not select X-axis. 1: Selects X-axis.
21	MAX1	Selects whether to include Y-axis in the target axis when “RMD.MSY = 11b”. For PCL6115, the selection is ignored. 0: Not select Y-axis. 1: Selects Y-axis.
22	MAX2	Selects whether to include Z-axis in the target axis when “RMD.MSY = 11b”. For PCL6115 and PCL6125, the selection is ignored. 0: Not select Z-axis. 1: Selects Z-axis.
23	MAX3	Selects whether to include U-axis in the target axis when “RMD.MSY = 11b”. For PCL6115 and PCL6125, the selection is ignored. 0: Not select U-axis. 1: Selects U-axis.
24	MSPE	Selects input function of CSTP terminal. You can stop own-axis by abnormal stop of other axes. 0: General-purpose input. CSTP terminal status can be obtained by RSTS.SSTP bit. 1: When a simultaneous stop signal is input, operation will decelerate & stop or stop immediately.
25	MSPO	Selects output function of CSTP terminal. You can stop other axes by abnormal stop of own-axis. 0: General-purpose output “One shot pulse” in negative logic can be output with CMSTP (07h) command. 1: Outputs one-shot pulse in negative logic at abnormal stop of own-axis.

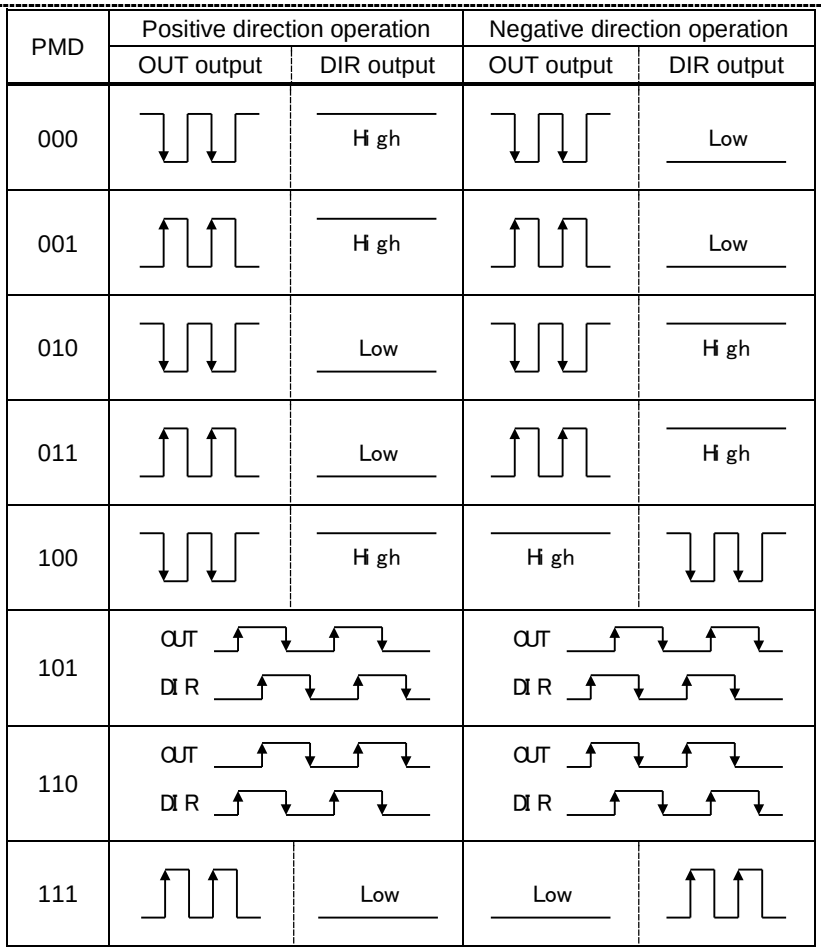
Position	Name	Description
26	MADJ	Selects triangular drive avoidance function 0: Avoid triangular drive. 1: Not avoid triangular drive.
27	(Undefined)	Always set “0”.
28	MCDE	Selects input functions of CSD terminal. You can decelerate own-axis at deceleration start of other axes. 0: General-purpose input CSD terminal status can be obtained by RSTS.SCSD bit. 1: Changes target speed to FL by inputting simultaneous slow-down signal.
29	MCDO	Selects output functions of CSD terminal. You can decelerate other axes at deceleration start of own-axis. 0: Not output “CSD = L level”. 1: Output “CSD = L level” during deceleration of own-axis and during FL constant speed operation.
31, 30	(Undefined)	Always set “0”.

4.4.4.2 RENV1: Environment setting 1 register

Register for environment setting 1. [WRENV1: 9Ch, RRENV1: DCh]

Sets mainly for I/O terminal specifications.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERCL	EPW			EROR	EROE	ALML	ALMM	ORGL	SDL	SDLT	SDM	ELM	PMD		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PMSK	PCSM	INTM	DTMF	DRF	FLTR	DRL	PCSL	LTCL	INPL	FTM		STPM	STAM	ETW	

Position	Name	Description
2 to 0	PMD	Selects output pulse mode.  The 90-degree phase difference signal output, 101b and 110b, are output with 4 multiplication.
3	ELM	Selects end-limit signal input process. [See Note.] 0: Immediate stop 1: Deceleration stop When deceleration stop is selected, deceleration starts with the input of the end limit signal in the direction of movement. Pays attention not to collide with mechanical systems etc. since it stops after passing through the end limit positions.

Position	Name	Description
4	SDM	Selects slow-down signal input process. [See Note.] 0: Deceleration only. 1: Deceleration stop.
5	SDLT	Selects input latch functions of SDn terminal. It can be used when the signal width of slow-down signal is short. 0: It does not latch input of slow-down signal. Status of the SDn terminal can be obtained with RSTS.SDIN bit. 1: It latches input of slow-down signal. Latch status can be obtained with RSTS.SSD bit. When SDn terminal is OFF at the start, latch status becomes OFF. Latch status can also be OFF by writing “RENV1.SDLT= 0”.
6	SDL	Selects input logic of SDn terminal. 0: Negative logic 1: Positive logic
7	ORGL	Selects input logic of ORGn terminal. 0: Negative logic 1: Positive logic
8	ALMM	Selects alarm signal input process. [See Note.] 0: Immediate stop 1: Deceleration stop
9	ALML	Selects ALMn terminal input logic. 0: Negative logic 1: Positive logic.
10	EROE	Selects output functions of ERCn terminal at abnormal stop. Deviation counter clear signal can be output when stopped by the input of PELn, MELn, ALMn and CEMG terminal input. Also stopped by CMEMG (05h) command. 0: Not output deviation counter clear signal. 1: Outputs deviation counter clear signal. However, it is not output during FL constant speed operation or decelerate stop at FL speed.
11	EROR	Selects output functions of ERCn terminal when returning to the origin position. The deviation counter clear signal can be output when origin-return is completed. 0: Not output deviation counter clear signal. 1: Output deviation counter clear signal.
14 to 12	EPW	Selects output pulse width of deviation counter clear signal. 000b: 11 to 13 µs 001b: 91 to 98 µs 010b: 360 to 390 µs 011b: 1.4 to 1.6 ms 100b: 11 to 13 ms 101b: 6 to 50 ms 110b: 93 to 100 ms 111b: Level output

Position	Name	Description
15	ERCL	Selects ERCn terminal output logic. 0: Negative logic 1: Positive logic
17, 16	ETW	Selects deviation counter clear signal OFF timer time. 00b: 0 µs, 01b: 11 to 13 µs, 10b: 1.4 to 1.6 ms, 11b: 93 to 100 ms
18	STAM	Selects simultaneous start signal input specification. 0: Level trigger 1: Edge trigger
19	STPM	Selects simultaneous stop signal input specification. [See Note.] 0: Immediate stop 1: Deceleration stop
21, 20	FTM	Selects the input noise filter characteristic of “RENV1.FLTR = 1”. 00b: 3.2 µs, 01b: 25 µs, 10b: 200 µs, 11b: 1.6 ms
22	INPL	Selects INPn terminal input logic. 0: Negative logic 1: Positive logic
23	LTCL	Selects counter latch signal specification. 0: Falling edge. 1: Rising edge. Depending on the input status of LTCn terminal, the value of counter may be latched when changing settings. See “7.10.2.1 Latch 1, 2” for details.
24	PCSL	Selects PCSn terminal input logic. 0: Negative logic 1: Positive logic
25	DRL	Selects PDRn, MDRn terminals input logic. 0: Negative logic 1: Positive logic
26	FLTR	Selects input noise filters for PELn, MELn, SDn, ORGn, ALMn, INPn and CEMG terminals. 0: Recognizes signals with pulse width of 0.1 µs or wider. 1: Recognizes signals whose pulse width is equal to or larger than the set value with RENV1.FTM bit.
27	DRF	Selects input nose filters for PDRn, MDRn and PEn terminals. 0: Recognizes signals with pulse width of 0.1 µs or wider. 1: Recognizes signals with pulse width of 54 ms or wider.
28	DTMF	Sets the direction change timer. 1: Wait for 0.2 ms after the direction change in the common pulse mode. 2: Wait for 0.5 µs after the direction change in the common pulse mode.

<table>
<tr><th>Position</th><th>Name</th><th>Description</th></tr>
<tr><td>29</td><td>INTM</td><td>Selects interrupt request signal output functions.
1: When an interrupt factor occurs, “INT = L level” is set.
2: When an interrupt factor occurs, “INT = L level” is not set
Main-status and interrupt factor register will change.</td></tr>
<tr><td>30</td><td>PCSM</td><td>Selects the functions of PCSn and STA terminals.
0: Functions selected by RMD.MPCS bit will be selected.
1: Own-axis start function will be selected.
It will not start even if simultaneous start signals are input to CSTA terminal.
<table>
<tr><th>RENV1.PCSM</th><th>RMD.MPCS</th><th>PCSn terminal</th><th>CSTA terminal</th></tr>
<tr><td>0</td><td>0</td><td>General-purpose input</td><td>Simultaneous start</td></tr>
<tr><td>0</td><td>1</td><td>Start pulse counts</td><td>Simultaneous start</td></tr>
<tr><td>1</td><td>0</td><td>Start own-axis</td><td>Shared input</td></tr>
</table></td></tr>
<tr><td>31</td><td>PMSK</td><td>Sets command pulse output functions.
0: Output
1: Not output
Counters will work.</td></tr>
</table>

Note: In the operations of FL and FH constant speed start, the axis stops immediately even if deceleration stop is selected.

4.4.4.3 RENV2: Environment setting 2 register

Register for environment setting 2. [WRENV2: 9Dh, RRENV2: DDh]

Sets mainly for terminal specifications of general purpose I/O port, encoder signal input, manual pulser signal input, and origin return controls.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POFF	EOFF	CSPO	P7M	P6M	P5M	P4M		P3M		P2M		P1M		P0M	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MRST	IEND	ORM	EZL	EZD				PDIR	PINF	PIM		EDIR	EINF	EIM	

Position	Name	Description
1 to 0	P0M	Selects the specification of P0n/FUPn terminals. 00b: General-purpose input 01b: General-purpose output 10b: Outputs acceleration signal with negative logic. 11b: Outputs acceleration signal with positive logic.
3 to 2	P1M	Selects the function of P1n/FDWn terminals 00b: General-purpose input 01b: General-purpose output 10b: Outputs slow-down signal with negative logic. 11b: Outputs slow-down signal with positive logic.
5 to 4	P2M	Selects the function of P2n/MVCn terminal. 00b: General-purpose input 01b: General-purpose output 10b: Outputs constant speed operating signal with negative logic. 11b: Outputs constant speed operating signal with positive logic.
7 to 6	P3M	Selects the function of P3/CP1 terminals. 00b: General-purpose input 01b: General-purpose output 10b: Outputs Comparator 1 condition satisfied signal with negative logic 11b: Outputs Comparator 1 condition satisfied signal with positive logic
9 to 8	P4M	Selects the function of P4n/CP2n terminals. 00b: General-purpose input 01b: General-purpose output 10b: Outputs Comparator 2 condition satisfied signal with negative logic. 11b: Outputs Comparator 2 condition satisfied signal with positive logic.
10	P5M	Selects the function of P5n terminals. 0: General-purpose input 1: General-purpose output

Position	Name	Description
11	P6M	Selects the function of P6n terminals. 0: General-purpose input 1: General-purpose output.
12	P7M	Selects the function of P7n terminals. 0: General-purpose input 1: General-purpose output
13	CSPO	Sets the function of CSTP terminal. Other axis can be stopped by stopping of own-axis by stop command. 0: A one-shot pulse with negative logic is not output when own-axis is stopped by stop command. 1: A one-shot pulse with negative logic is output when own-axis is stopped by stop command. The condition is “RMD.MSPO =1”.
14	EOFF	Sets the input function of EAn, EBn terminals. 0: Encoder signal input is enabled 1: Encoder signal input is disabled It also does not detect input errors.
15	POFF	Sets the input function of PAn, PBn terminals. 0: Manual pulser signal input is enabled. 1: Manual pulser signal input is disabled. It also does not detect input errors.
17, 16	EIM	Selects the input specification of encoder signals(EAn, EBn). 00b: 90-degree phase difference mode of 1 multiplication. 01b: 90-degree phase difference mode of 2 multiplication 10b: 90-degree phase difference mode of 4 multiplication 11b: 2-pulse mode See “7.10.1 Counter type and input specification” for details.
18	EINF	Selects the noise filter of EAn, EBn, and EZn terminals. 0: It recognizes signals with a pulse width of 0.1 μs or wider. 1: It recognizes signals with a pulse width of 0.15 μs or wider.
19	EDIR	Selects the counting directions of encoder signals (EAn, EBn). 0: Forward direction 1: Reversed direction
21, 20	PIM	Selects the input specification of manual pulser signal (PAn, PBn). 00b: 90-degree phase difference mode of 1 multiplication. 01b: 90-degree phase difference mode of 2 multiplication. 10b: 90-degree phase difference mode of 4 multiplication. 11b: 2-pulse mode. See “5.3 Manual pulser control” for details

Position	Name	Description
22	PINF	Selects input noise filter of PAn and PBn terminals. 0: Recognizes signals with pulse width of 0.1 µs or wider. 1: Recognizes signals with pulse width of 0.15 µs or wider.
23	PDIR	Selects the counting directions of manual pulser signals (PAn, PBn). 0: Forward direction 1: Reversed direction
27 to 24	EZD	Sets the count value of encoder Z-phase signal used for origin return control. The setting range is 0000b (1st time) to 1111b (16th time).
28	EZL	Selects the input specifications of encoder Z-phase signal. 0: Falling edge. 1: Rising edge
29	ORM	Selects the operation mode of origin return control using encoder Z-phase signal. 0: Operation mode of origin return 0; it does not use encoder Z-phase signal. At constant speed start, it will immediately stop when origin signal turns ON from OFF. At high-speed start, it decelerates and stops when origin signal turns ON from OFF. Counter clear timing is when origin signal input turns ON from OFF. 1: Operation mode of origin return 1; it uses encoder Z-phase signals. At constant speed start, an operation stops at the input of specified number of encoder Z-phase signals after origin signal turns ON from OFF. At high-speed start, deceleration starts when origin signal turns ON from OFF, and operation stops when the specified number of encoder Z-phase signals is input. Counter clear timing is when specified number of encoder Z-phase signals is input.
30	IEND	Selects stop interrupt (MSTS.SENI) function: 0: No stop interrupt function 1: Stop interrupt generates “INT = L level” when stopped regardless of normal stop or abnormal stop.
31	MRST	Selects a method to clear bits of various interrupt factors (MSTS.SENI, REST, and RIST) and a bit indicating a stop other than a target position (MSTS.SEOR). 0: Automatic clear by reading 1: Manual clear by writing It can be cleared by SENIR (2Dh) command, SEORR (2Eh) command, and writing the corresponding bit to REST register and RIST register. In the case of serial bus interface, it is fixed to “RENV2.MRST = 1” (manual clear by writing).

4.4.4.4 RENV3: Environment setting 3 register

Register for environment setting 3. [WRENV3: 9Eh, RRENV3: DEh]

Mainly sets counter functions, latch 1 and 2 functions, comparator functions and internal synchronous signal I/O functions.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2S		C1S		C2RM	CU2R	LOF2	CU2L	C1RM	CU1R	LOF1	CU1L	CU2H	CU1H	CIS2	CIS1
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	SLCU	SLM		SYI		SYO			

Position	Name	Description
0	CIS1	Selects the counting target of Counter 1 (RCUN1). 0: Command position (Command pulse) 1: Mechanical position (Encoder signal)
1	CIS2	Selects the counting target of Counter 2 (RCUN2). 0: Mechanical position (Encoder signal) 1: Command position (Command pulse)
2	CU1H	Sets counting function of Counter 1 (RCUN1). 0: Counts the target. 1: Not count the target.
3	CU2H	Sets counting function of Counter 2 (RCUN2). 0: Counts the target. 1: Not count the target.
4	CU1L	Sets Counter 1 (RCUN 1) clear function at the same time as latching to RLTC1 register. 0: Not clear Counter 1. 1: Clears Counter 1.
5	LOF1	Sets the latch function to RLTC1 register by LTCn terminal. 0: Latches counter 1 by counter latch signal input. 1: Not latch counter 1 by counter latch signal input. It can be latched by LTCH (29h) command. Counter latch signal is “edge-trigger”.
6	CU1R	Sets the latch function to RLTC1 register by origin-return control. 0: Not latch counter 1 by origin return control. 1: Latches counter 1 by origin return control.
7	C1RM	Sets the ring counter function of counter 1 (RCUN 1). 0: Not perform a ring counter operation using Comparator 1. 1: Performs a ring counter operation using Comparator 1.
8	CU2L	Sets counter 2 (RCUN 2) clear function at the same time as latching to RLTC2 register. 0: Not clear counter 2. 1: Clears counter 2.

Position	Name	Description
9	LOF2	Sets the latch function to RLTC2 register by LTCn terminal. 0: Latches counter 2 with counter latch signal input. 1: Not latch counter 2 with counter latch signal input. It can be latched by LTCH (29h) command. Counter latch signal is the edge-trigger.
10	CU2R	Sets the latch function to RLTC2 register by origin return control. 0: Not latch counter 2 with origin return control. 1: Latches Counter 2 with origin return control.
11	C2RM	Sets the ring counter function of counter 2 (RCUN 2). 0: Not perform a ring counter operation using Comparator 2. 1: Performs a ring counter operation using Comparator 2.
13 to 12	C1S	Selects the comparison method for Comparator 1. 00b: Not use Comparator 1 (=Not compare). 01b: RCMP1 register value = RCUN1 register value 10b: RCMP1 register value > RCUN1 register value 11b: RCMP1 register value < RCUN1 register value
15 to 14	C2S	Selects a comparison method for Comparator 2. 00b: Not use Comparator 2. 01b: RCMP2 register value = RCUN2 register value 10b: RCMP2 register value > RCUN2 register value 11b: RCMP2 register value < RCUN2 register value
19 to 16	SYO	Selects the output condition for the internal synchronous signal. 0001b: Comparator 1 condition is met. 0010b: Comparator 2 condition is met. 1000b: Starts acceleration. 1001b: Ends acceleration. 1010b: Starts deceleration. 1011b: Ends deceleration. Others: Not output an internal synchronous signal.
21, 20	SYI	Selects the input target of internal synchronous signals. 00b: Internal synchronous signal output by X-axis. 01b: Internal synchronous signal output by Y-axis. 10b: Internal synchronous signal output by Z-axis. 11b: Internal synchronous signal output by U-axis
23, 22	SLM	Selects the process of software limit function. 00b: Not stop at the software limit position; No interrupt occurs. 01b: Not stop at the software limit position; Event interrupt occurs. 10b: Stops immediately at the software limit position; Error interrupt occurs. 11b: Decelerates and stops at the software limit position; Error interrupt occurs.
24	SLCU	Selects the counter to manage software limits. 0: Selects COUNTER 1 (RCUN1) 1: Selects COUNTER 2 (RCUN2)
31 to 25	(Un-defined)	Always set “0”.

4.4.4.5 RENV4: Environment setting 4 register

Register for environment setting 4. [WRENV4: 9Fh, RRENV4: DFh]

Mainly sets latch 3 and 4 functions.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L4F		L4MD	L4DT	L4TL	L4T			L3F		L3MD	L3DT	L3TL	L3T		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Position	Name	Description
2 to 0	L3T	Selects the input terminal of a trigger signal to be latched in RLTC3 register. 000: Disable 001: LTCn terminal 010: ORGn terminal 011: EZn terminal 100: P4n terminal 101: P5n terminal 110: P6n terminal 111: P7n terminal
3	L3TL	Select the input specification of trigger signals to be latched in RLTC3 register. [Note] 0: Falling edge. 1: Rising edge
4	L3DT	Selects the counter to be latched in the RLTC3 register. 0: Selects Counter 1(RCUN1). 1: Selects Counter 2(RCUN2).
5	L3MD	Selects latch operation specification of RLTC3 register. 0: Latches with only the first trigger signal. 1: Latches with every trigger signal.
7, 6	L3F	Selects the input noise filter characteristic of a trigger signal to be latched in the RLTC3 register. 00b: Recognizes a signal with a pulse width of 0.1 µs or more. 01b: Recognizes signals with a pulse width of 3.2 µs or more. 10b: Recognizes signals with a pulse width of 25 µs or more. 11b: Recognizes signals with a pulse width of 200 µs or more. In addition, it is not related to setting of RENV1.FLTR bit or RENV2.EINF bit.
10 to 8	L4T	Selects the input terminal of a trigger signal to be latched in the RLTC4 register. 000: Disable 001: LTCn terminal 010: ORGn terminal 011: EZn terminal 100: P4n terminal 101: P5n terminal 110: P6n terminal 111: P7n terminal
11	L4TL	Select the input specification of trigger signals to be latched in RLTC4 register. [Note] 0: Falling edge. 1: Rising edge
12	L4DT	Selects the counter to be latched in the RLTC4 register. 0: Selects Counter 1(RCUN1) 1: Selects Counter 2(RCUN2).
13	L4MD	Selects latch operation specification of RLTC4 register. 0: Latches with only the first trigger signal. 1: Latches with every trigger signal.

Position	Name	Description
15, 14	L4F	Selects the input noise filter characteristic of a trigger signal to be latched in the RLTC4 register. 00b: Recognizes a signal with a pulse width of 0.1 µs or more. 01b: Recognizes signals with a pulse width of 3.2 µs or more. 10b: Recognizes signals with a pulse width of 25 µs or more. 11b: Recognizes signals with a pulse width of 200 µs or more. In addition, it is not related to setting of RENV1.FLTR bit or RENV2.EINF bit.
31 to 16	(Un-defined)	Always set “0”.

Note: After changing the input specification (RENV4.L3TL) of a trigger signal latched in the RLTC3 register, be sure to wait for the set time of the input noise filter characteristic (RENV4.L3F) before writing LTC3E (3Ch) command.
If the LTC3E (3Ch) command is written before the setting time of input noise filter characteristic (RENV4.L3F) completes, extra latch operation will occur.
If you change the trigger signal input specification (RENV4.L3TL) after setting “RENV4.L3TL = 00b”, and set it to arbitrary input noise filter characteristics, the waiting time becomes unnecessary due to register write time.
This also applies to the trigger signal input specification (RENV4.L4TL) latched in the RLTC4 register.

4.4.4.6 RGPM: Shared I/O port management register

Register to manage shared I/O ports. [WRGPM: BAh, RRGPM: FAh]

Selects the function specifications of shared I/O ports (GP0 to GP15) that can be used with the serial bus interface.

It will be ignored with pararell interface.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GM15	GM14	GM13	GM12	GM11	GM10	GM9	GM8	GM7	GM6	GM5	GM4	GM3	GM2	GM1	GM0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Position	Name	Description
15 to 0	GM15 to GM0	Select function specifications of GP15 to GP0 terminals. 0: Select input port 1: Select output port
31 to 16	(Undefined)	Always set “0”.

4.4.4.7 RGPD: Shared I/O port information register

Register to set and get status of shared I/O port. [WRGPD: BBh, RRGPD: FBh]

Sets or gets status of shared I/O ports (GP0 to GP15) that can be used with serial bus interface.

I/O port status can be read.

Output status of output port can be written.

It will be ignored with pararell interface.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GD15	GD14	GD13	GD12	GD11	GD10	GD9	GD8	GD7	GD6	GD5	GD4	GD3	GD2	GD1	GD0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Position	Name	Description
15 to 0	GD15 to GD0	When reading, the status of GP15 to GP0 can be obtained. When writing, the output status of GP15 to GP0 can be set. 0: Obtains or sets L level. 1: Obtains or sets H level.
31 to 16	(Undefined)	Always set “0”.

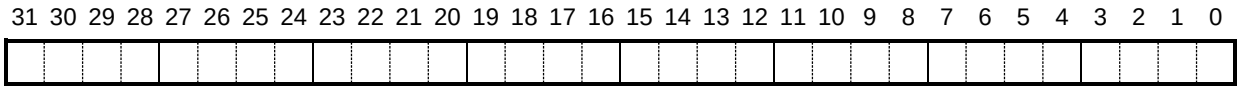
4.4.5 Count register

The following is the registers for counters:

No.	Name	Description	Bit length	Range	R/W
1.	RCUN1	Counter 1(Mainly command position)	32	-2,147,483,648 to +2,147,483,647	R/W
2.	RCUN2	Counter 2(Mainly mechanical position)	32	-2,147,483,648 to +2,147,483,647	R/W
3.	RCMP1	Comparison data 1	32	-2,147,483,648 to +2,147,483,647	R/W
4.	RCMP2	Comparison data 2	32	-2,147,483,648 to +2,147,483,647	R/W
5.	RCMP3	Comparison data 3 (Only for software limit)	32	-2,147,483,648 to +2,147,483,647	R/W
6.	RCMP4	Comparison data 4 (Only for software limit)	32	-2,147,483,648 to +2,147,483,647	R/W
7.	RLTC1	Latch data 1 (Only for counter 1)	32	-2,147,483,648 to +2,147,483,647	R
8.	RLTC2	Latch data 2 (Only for counter 2)	32	-2,147,483,648 to +2,147,483,647	R
9.	RLTC3	Latch data 3	32	-2,147,483,648 to +2,147,483,647	R
10.	RLTC4	Latch data 4	32	-2,147,483,648 to +2,147,483,647	R

4.4.5.1 RCUN1: Counter 1 register

Register to set and get the status of Counter 1. [WRCUN1: A3h, RRCUN1: E3h]

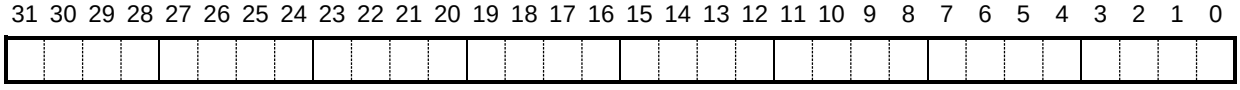


Setting range: −2,147,483,648 to +2,147,483,647

See “7.10 Counters” for details.

4.4.5.2 RCUN2 : Counter 2 register

Register to set and get status of Counter 2. [WRCUN2: A4h, RRCUN2: E4h]

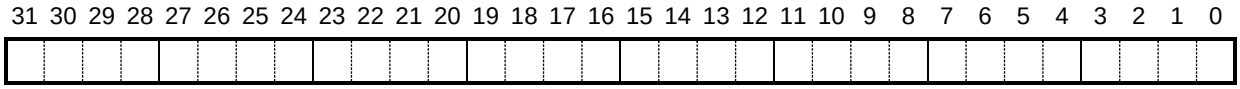


Setting range: −2,147,483,648 to +2,147,483,647

See “7.10 Counters” for details.

4.4.5.3 RCMP1: Comparison data 1 register

Sets and gets status of comparison data 1. [WRCMP1: A7h, RRCMP1: E7h]

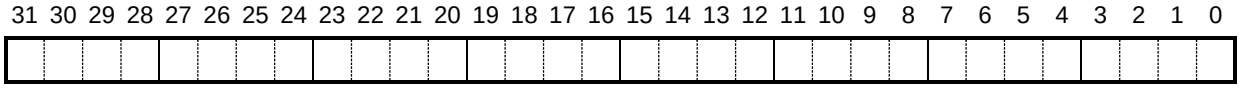


Setting range: −2,147,483,648 to +2,147,483,647

See “7.11 Comparators” for details.

4.4.5.4 RCMP2: Comparison data 2 register

Sets and gets status of comparison data 2. [WRCMP2: A8h, RRCMP2: E8h]

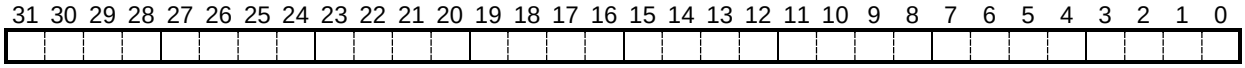


Setting range: −2,147,483,648 to +2,147,483,647

See “7.11 Comparators” for details.

4.4.5.5 RCMP3: Comparison data 3 register

Sets and gets status of comparison data 3. [WRCMP3: A9h, RRCMP3: E9h]
Only for software limit function.

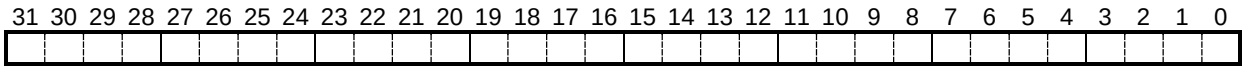


Setting range: −2,147,483,648 to +2,147,483,647

See “7.11 Comparators” for details.

4.4.5.6 RCMP4: Comparison data 4 register

Sets and gets status of comparison data 4. [WRCMP4: AAh, RRCMP4: EAh]
Only for software limit function.

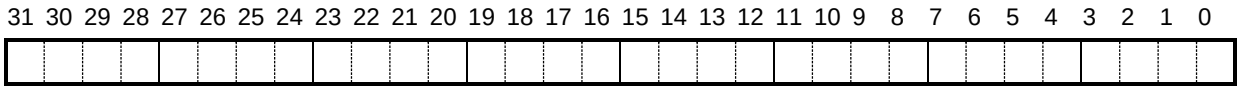


Setting range: −2,147,483,648 to +2,147,483,647

See “7.11 Comparators” for details.

4.4.5.7 RLTC1: Latch data 1 register

Register to obtain latch data 1. [RRLTC1: EDh]
Only for counter 1(RCUN1).

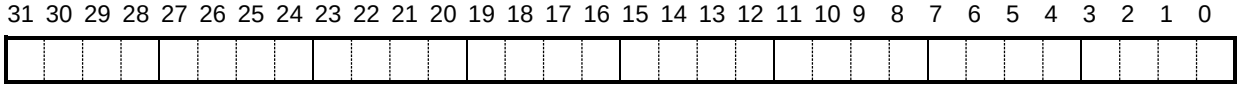


Data range: –2,147,483,648 to +2,147,483,647

See “7.10.2 Latch and clear (LTCn)” for details.

4.4.5.8 RLTC2: Latch data 2 register

Register to obtain latch data 2. [RRLTC2: EEh]
Only for counter 2(RCUN2).

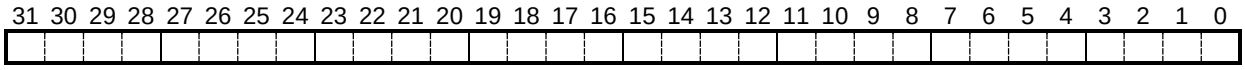


Data range: –2,147,483,648 to +2,147,483,647

See “7.10.2 Latch and clear (LTCn)” for details.

4.4.5.9 RLTC3: Latch data 3 register

Register to obtain latch data 3. [RRLTC3: EFh]

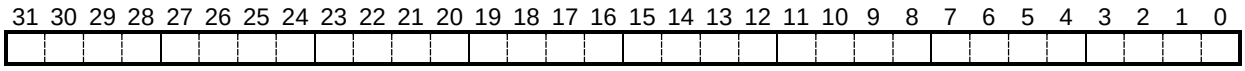


Data range: –2,147,483,648 to +2,147,483,647

See “7.10.2 Latch and clear (LTCn)” for details.

4.4.5.10 RLTC4: Latch data 4 register

Register to obtain latch data 4 [RRLTC4: F0h]



Data range: –2,147,483,648 to +2,147,483,647

See "7.10.2 Latch and clear (LTCn)” for details.

4.4.6 Interrupt register

The following shows the registers for interrupt settings.

No.	Name	Description	Length	Range	R/W
1.	RIRQ	Sets event interrupt factor	18	-	R/W
2.	REST	Obtains error interrupt factor	11	-	R/W
3.	RIST	Obtains event interrupt factor	20	-	R/W

4.4.6.1 RIRQ: Event interrupt factor setting register

Register to set and obtain the event interrupt factor setting. [WRIRQ: ACh, RRIRQ: ECh]
Sets the bit corresponding to the content to generate an event interrupt to “1”.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	IRBY	IREZ	IRSA	IRDR	IRSD	IROL	IRLT	IRC2	IRC1	IRDE	IRDS	IRUE	IRUS	IRNM	IREN
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	IRL4	IRL3

Position	Name	Description
0	IREN	1: If stopped normally, an interrupt is generated.
1	IRNM	1: If the pre-register changes to be enabled to write, an interrupt is generated.
2	IRUS	1: When acceleration starts, an interrupt is generated.
3	IRUE	1: When acceleration is completed, an interrupt is generated.
4	IRDS	1: When deceleration starts, an interrupt is generated.
5	IRDE	1: When deceleration is completed, an interrupt is generated.
6	IRC1	1: When comparator 1 condition is met, an interrupt is generated.
7	IRC2	1: When comparator 2 condition is met, an interrupt is generated.
8	IRLT	1: Interrupt is generated by latching the count value with input of a counter latch signal. The target is RLTC1 register or RLTC2 register. When both “RENV3.LOF1 = 1” and “RENV3.LOF2 = 1” are set, no interrupt is generated.
9	IROL	When the origin signal turns ON, an interrupt is generated. When both “RENV3.CU1R = 0” and “RENV3.CU2R = 0” are set, no interrupt is generated. This interrupt can be generated in operation modes other than the origin return control.
10	IRSD	When slow-down signal turns ON, an interrupt is generated This interrupt is also generated with setting “RMD.MSDE = 0”.
11	IRDR	1: An interrupt is generated if the input to PDRn terminal or MDRn terminal changes. This interrupt is not generated when “PEn = H level”. This interrupt is also generated in operation modes other than switch control.
12	IRSA	1: An interrupt is generated when it becomes “CSTA = L level”.
13	IREZ	1: When stopped during deceleration with “RENV2.ORM = 1”, an interrupt is generated.
14	IRBY	1. When starting, an interrupt is generated.

Position	Name	Description
15	(Undefined)	Always set “0”.
16	IRL3	1: If the count value is latched in RLTC3 register, an interrupt is generated.
17	IRL4	1: If the count value is latched in RLTC4 register, an interrupt is generated.
31 to 18	(Undefined)	Always set “0”.

4.4.6.2 REST: Error interrupt factor obtaining register

Register to obtain the error interrupt factor. [WREST: B2h, RREST: F2h]
The corresponding bit will be “1” when an error interrupt occurs.
When “RENV2.MRST = 0” is set, all bits are cleared by reading REST register.
When “RENV2.MRST = 1” is set, only corresponding bit is cleared by writing “1” to a bit that you want to clear.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	ESMS	ESPS	ESPE	ESEE	ESPO	ESSD	ESEM	ESSP	ESAL	ESML	ESPL
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Position	Name	Description
0	ESPL	1: Stopped by turning end limit signal in positive direction ON.
1	ESML	1: Stopped by turning end limit signal in negative direction ON.
2	ESAL	1: Stopped by turning alarm signal ON or an alarm signal turns ON while stopping.
3	ESSP	1: Stopped by turning simultaneous stop signal ON.
4	ESEM	1: Eemergency stop signal turns ON or writing CMEMG (05h) command.
5	ESSD	1: Stopped by turning slow-down signal ON.
6	ESPO	1: Stopped by an overflow occurred in the manual pulser buffer counter.
7	ESEE	1: Encoder signal input error occurred. An input error occurs when signals of EAn and EBn terminals change at the same time in 90-degree phase difference mode, or when signals of EAn and EBn terminals rise at the same time in 2-pulse mode.
8	ESPE	1: Manual pulser signal input error occurred. An input error occurs when the signals of PAn and PBn terminal rise at the same time.
9	ESPS	Stopped by detecting software limit in positive direction. It occurs when “RENV3.SLM = 10b” or “RENV3.SLM = 11b”.
10	ESMS	Stopped by detecting software limit in negative direction. It occurs when “RENV3.SLM = 10b” or “RENV3.SLM = 11b”.
31 to 11	(Undefined)	It is always “0”.

4.4.6.3 RIST register

Register to obtain the event interrupt factor [WRIST: B3h, RRIST: F3h]
The corresponding bit will be “1” when an error interrupt occurs.
When “RENV2.MRST = 0” is set, all bits are cleared by reading RIST register.
When “RENV2.MRST = 1” is set, only corresponding bit is cleared by writing “1” to a bit to reset.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISMS	ISPS	ISSA	ISMD	ISPD	ISSD	ISOL	ISLT	ISC2	ISC1	ISDE	ISDS	ISUE	ISUS	ISNM	ISEN
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	ISL4	ISL3	ISBY	ISEZ

Bit	Bit name	Description
0	ISEN	1: When stopped normally.
1	ISNM	1: When writing to pre-register is enabled.
2	ISUS	1: When acceleration starts.
3	ISUE	1: When acceleration is completed.
4	ISDS	1: When deceleration starts.
5	ISDE	1: When deceleration is completed.
6	ISC1	1: When comparator 1 condition is met.
7	ISC2	1: When comparator 2 condition is met.
8	ISLT	1: When the count value is latched by a counter latch signal input.
9	ISOL	1: When the origin signal turns ON.
10	ISSD	1: When the slow-down signal turns ON.
11	ISPD	1: When the input of positive side switch signal is changed.
12	ISMD	1: When the input of negative side switch signal is changed.
13	ISSA	1: When it becomes “CSTA = L level”.
14	ISPS	1: Detecting the positive side software limit. Generated only when “RENV3.SLM1 = 01b”.
15	ISMS	1: Detecting the negative side software limit. Generated only when “REV3.SLM1 = 01b”.
16	ISEZ	1: Stopped during deceleration with “RENV2.ORM = 1”.
17	ISBY	1: Started.
18	ISL3	1: The count value is latched in RLTC3 register.
19	ISL4	1: The count value is latched in RLTC4 register.
31 to 20	(Undefined)	It is always “0”.

4.4.7 Status indicating register

Register to indicate status.

No.	Name	Description	Length	Range	R/W
1.	RSTS	Obtains extension status	23	-	R

4.4.7.1 RSTS: Obtaining extension status register

Register to obtain extended status. [RRSTS: F1h]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SINP	SDIN	SLTC	SMDR	SPDR	SEZ	SERC	SPCS	SEMG	SSTP	SSTA	SCSD	CND			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	SL4F	SL4C	SL4E	SL3F	SL3C	SL3E	SDIR

Position	Name	Description
3 to 0	CND	Indicate operation status. 0000b: While stopping 0001b: Waiting for external switch signal. 0010b: Waiting for simultaneous start signal 0011b: Waiting for internal synchronous signal 0100b: Waiting for target axis to stop 0101b: Waiting for completion of deviation counter clear signal OFF timer. 0110b: Waiting for completion of direction change timer 1000b: Waiting for manual pulser signal input 1010b: Operating at FL constant speed. 1011b: Accelerating 1100b: Operating at FH constant speed. 1101b: Decelerating 1110b: Waiting for input of in-position signal Others: Controlling start/stop Note: “Others” status will be changed to other status after inputting CLK signals several times.
4	SCD	1: “CSD = L level”.
5	SSTA	1: “CSTA = L level”.
6	SSTP	1: “CSTP = L level”.
7	SEMG	1: “CEMG = L level”.
8	SPCS	1: “PCSn = L level” when “RMD.PCSL = 0”. “PCSn = H level” when “RMD.PCSL = 1”.
9	SERC	1: “ERCn = L level” when “RMD.ERCL = 0”. “ERCn = H level” when “RMD.ERCL = 1”.
10	SEZ	1: “EZn = L level”.
11	SDRP	1: “PDRn = L level” when “RMD.DRL = 0”. “PDRn = H level” when “RMD.DRL = 1”.

Position	Name	Description
12	SDRM	1: “MDRn = L level” when “RMD.DRL = 0”. “MDRn = H level” when “RMD.DRL = 1”.
13	SLTC	1: “LTCn = L level” when “RENV1.LTCL = 0”. “LTCn = H level” when “RENV1.LTC = 1”.
14	SDIN	1: “SDn = L level” when “RMD.SDL = 0”. “SDn = H level” when “RMD.SDL = 1”. Slow-down latch signal can be obtained with SSTS.SSD bit.
15	SINP	1: “INPn = L level” when “RMD.INPL = 0”. “INPn = H level” when “RMD.INPL = 1”.
16	SDIR	0: Operation in positive direction. 1: Operation in negative direction.
17	SL3E	0: The trigger signal for latching RLTC3 register is not monitored. 1: The trigger signal for latching RLTC3 register is monitored. Sets by LTC3E (3Ch) command.
18	SL3C	0: Not latched with RLTC3 register. 1: Latched more than once with RLTC3 register. Clear by LTC3D (3Eh) command.
19	SL3F	Each time RLTC3 register value is changed, it toggles to change. Clear with LTC3D (3Eh) command.
20	SL4E	0: The trigger signal for latching RLTC4 register is not monitored. 1: The trigger signal for latching RLTC4 register is monitored. Sets by LTC4E (3Dh) command.
21	SL4C	0: Not latched with RLTC4 register. 1: Latched more than once with RLTC4 register. Clear by LTC4D (3Fh) command.
22	SL4F	Each time RLTC4 register value is changed, it toggles to change. Clear with LTC4D (3Fh) command.
31 to 23	(Undefined)	It is always “0”.

5. Operation Mode

Sets the basic operation mode using the mode selection bit “RMD.MOD” in operation mode setting register.

5.1 Command control

Writing start command starts an operation mode.

Writing stop command stops an operation mode.

When the output pulse mode is common pulse mode or 2-pulse mode, the direction signal changes at the time of writing the RMD register.

MOD	Operation mode	Direction of movement
00h	Continuous movement in positive direction.	Positive (+) direction
08h	Continuous movement in negative direction.	Negative (−) direction

5.1.1 Positive direction continuous movement operation mode (MOD: 00h)

The command pulse is continuously output in positive direction according to the setting of speed control registers in this operation mode. This operation mode can be ended by writing stop commands.

Speed controls can be made freely during operation by using target speed override functions and speed change commands.

5.1.2 Negative direction continuous movement operation mode (MOD: 08h)

The command pulse is continuously output in negative direction according to the setting of speed control registers in this operation mode. This operation mode can be ended by writing stop commands.

Speed controls can be made freely during operation by using target speed override functions and speed change commands.

5.2 Positioning control

Writing start command starts the operation mode.

It stops its operation mode when it reaches the target position.

MOD	Operation mode	Direction of movement
41h	Incremental movement	Positive direction when PRMV ≥ “0”. Negative direction when PRMV < “0”.
47h	Timer operation	Positive direction (“DIR terminal= H level”). However, any pulses are not output.

5.2.1 Incremental movement operation mode (MOD: 41h)

It is an operation mode to move relatively to the target position set in RMV register.

A sign of the RMV register determines operating direction.

When starting, the RMV register absolute value is loaded into the RPLS register.

RPLS register counts down per every command pulse output, and operation stops and ends when “RPLS = 0”.

When you set “RMV = 0” and start an operation mode, the axis will stop immediately without outputting any command pulses.

5.2.2 Timer operation mode (MOD: 47h)

This operation mode allows an operation time to be used as a timer.

The internal effect of this operation mode is identical to an incremental movement operation mode; however, no pulse is output. The operation time when using STAFH (51h) command is the product of command pulse output cycle and the RMV register value. (e.g. it becomes 120 ms when the FH speed by the RFH register value and RMG register value is 1000 pps and the RMV register value is 120 pulses). Write a positive number (1 to 2,147,483,647) into the PRMV register.

Inputs of positive side end limit signal, negative side end limit signal, slow-down signal, or alarm signal, and software limit will not cause abnormal stops.

Inputting of simultaneous stop signal or emergency stop signal will cause an abnormal stop.

The direction change timer does not work. The command position counter does not count.

Regardless of the input function setting (RMD.MINP) of the in-position signal, operation completion delay due to the in-position signal does not occur.

Sets the operation completion timing to “RMD.METM = 0” (output pulse cycle completion) in order to reduce the error of operation time. Even with cycle completion, it takes 15 cycles (0.75 μs) of the longest CLK signal for internal processing from start to stop. Therefore, it may take up to 750 ns longer than the set time.

5.3 Manual pulser control

It operates in synchronization with the input of manual pulser signals (PAn, PBn).

It can be used when “PEn = L level” and “RENV2.POFF = 0”.

Using PEn terminal, you can switch to use one manual pulser for multiple axes.

An input noise filter of PEn terminals can be selected (RENV1.DRF).

An input noise filters of PAn and PBn terminals can also be selected (RENV2.PINF).

When start command is written, the operation status becomes “RSTS.CND = 1000b”.

After that, when a manual pulser signal is input to PAn terminal or PBn terminal, command pulses are output from OUTn and DIRn terminals. For start command, use STAFH (51h) command.

The input specification of manual pulser signals can be selected from 4 types with RENV2.PIM bit:

• 90-degree phase difference signal of 1 multiplication

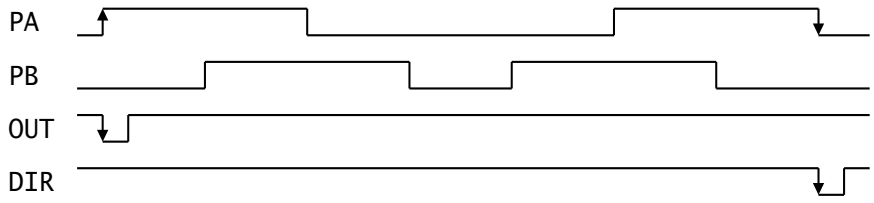
• 90-degree phase difference signal of 2 multiplication

• 90-degree phase difference signal of 4 multiplication

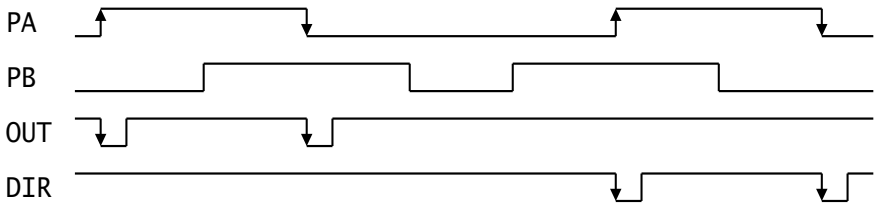
• 2-pulse signal (positive direction pulse and negative direction pulse)

The followings are examples of operation timing when 2-pulse mode (RENV1.PMD = 100b) is set for outputs of OUTn and DIRn terminals:

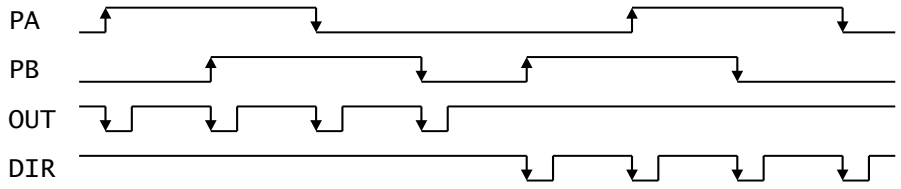
1) When using input of 90-degree phase difference signal of 1 multiplication (RENV2.PIM = 00b)



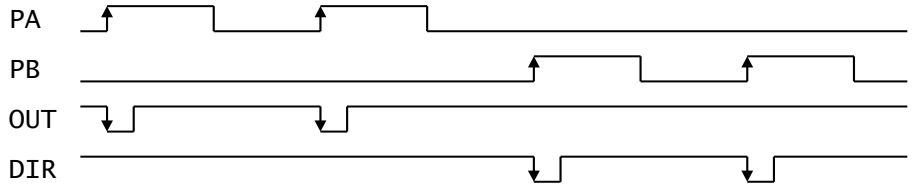
2) When using input of 90-degree phase difference signal of 2 multiplication (RENV2.PIM = 01b)



3) When using input of 90-degree phase difference signal of 3 multiplication (RENV2.PIM = 10b)



4) When using 2-pulse signal input. (RENV2.PIM = 11b)



In synchronization with an input of manual pulser signals, internal pulse of FH speed is output intermittently.

Therefore, between input of manual pulser signal and output of command pulse, an error of one internal pulse cycle can occur at the longest.

Be sure to use the “maximum input frequency (FP)” of manual pulser signal below FH speed.

$$\text{Maximum input frequency (FP)} < \frac{\text{FH speed}}{\text{Input interface multiplied value}}$$

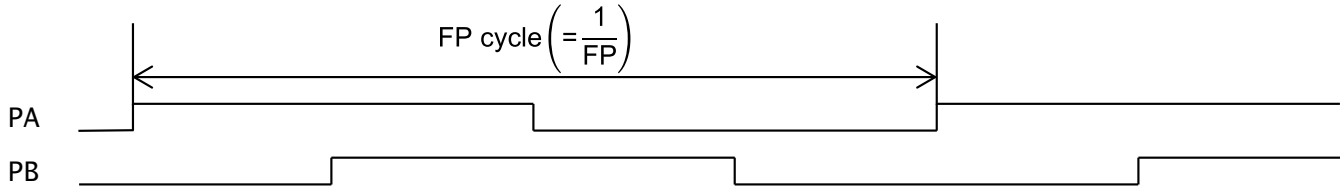
“Input interface multiplying value” in two-pulse input is “1”, the same value as “90-degree phase difference of 1 multiplication”.

Input specification of manual pulser signal	Input interface multiplication value
90-degree phase difference of 1 multiplication	1
90-degree phase difference of 2 multiplication	2
90-degree phase difference of 4 multiplication	4
2-pulse signal	1

An error interrupt (REST.ESPO) is generated when input buffer counter (signed 4 bit) overflows at an input frequency of FP or more.

An error interrupt (REST.ESPE) is generated if the signals of PAn terminal and PBn terminal rise at the same time.

Example: When “FH speed = 1000 pps” with input of 90-degree phase difference of 2 multiplication, the input frequency of manual pulser signals is less than 500 Hz.



Remark: If a manual pulser input frequency fluctuates, set the shortest cycle to the above “FP cycle”.

Input specification of manual pulser signal (PAn, PBn) <RENV2.PIM(21, 20)> 00b: 90-degree phase difference mode of 1 multiplication 01b: 90-degree phase difference mode of 2 multiplication10b: 90-degree phase difference mode of 4 multiplication 11b: 2- pulse mode	[RENV2] (R/W) 23 16 - - n n - - - -
Counting direction of manual pulser signal (PAn, PBn) <RENV2.PDIR(23)> 0: Forward rotation. 1: Reverse rotation.	[RENV2] (R/W) 23 16 n - - - - - - -
Input function of manual pulser signal (PAn, PBn) input function <RENV2.POFF(15)> 0: Enables manual pulser input. 1: Disables manual pulser input. Input errors are not detected.	[RENV2] (R/W) 15 8 n - - - - - - -
Input noise filter (PEn, PDRn, MDRn) <RENV1.DRF(27)> 0: Recognizes signals with pulse width of 0.1 µs or wider. 1: Recognizes signals with pulse width of 54 ms or wider.	[RENV1] (R/W) 31 24 - - - - n - - -
Input noise filter (PAn, PBn) <RENV2.PINF(22)> 0: Recognizes signals with pulse width of 0.1 µs or wider. 1: Recognizes signals with pulse width of 0.15 µs or wider.	[RENV2] (R/W) 23 16 - n - - - - - -
Obtaining operation status <RSTS.CND(3 to 0)> 1000b: Waits for manual pulse signal input.	[RSTS] (R) 7 0 - - - - n n n n
Obtaining error interrupt factor <REST.ESPE(8)> 1: A manual pulser signal input error occurs. An input error occurs if the signals of PAn and PBn terminals rise at the same time.	[REST] (R/W) 15 8 0 0 0 0 0 - - n
Obtaining error interrupt factor <REST.ESPO(6)> 1: Stopped due to buffer counter overflow of manual pulser signal.	[REST] (R/W) 7 0 - n - - - - - -

The pulser control has the following 2 operation modes:

MOD	Operation mode	Direction of movement
01h	Continuous movement	Determined by manual pulser signal input.
51h	Incremental movement	Movement in positive (+) direction when RMV ≧ 0. Movement in negative (−) direction when RMV < 0.

5.3.1 Continuous movement operation mode (MOD: 01h)

It is an operation mode to move continuously in synchronization with the input of manual pulser signals.

The operation mode can be ended by writing STOP (49h) command.

Setting 1 to RENV2.PDIR bit can reverse the direction of operation without changing the wiring of PAn and PBn terminals.

Manual pulser signal input specification	PDIR	Operating direction	A-phase /B-phase signal input
90-degree phase difference signal (1, 2, and 4 multiplication)	0	(+) direction	When A-phase leads B-phase.
		(−) direction	When B-phase leads A-phase.
	1	(+) direction	When B-phase leads A-phase.
		(−) direction	When A-phase leads B-phase.
2-pulse input (+) direction pulse and (−) direction pulse	0	(+) direction	A-phase input rising edge.
		(−) direction	B-phase input rising edge.
	1	(+) direction	B-phase input rising edge.
		(−) direction	A-phase input rising edge.

An operation stops when an end limit signal in the current operating direction turns ON, but it can re-start and operate in the opposite direction without writing a start command again.

No error interrupt occurs when an operation stops by end limit input in the current operating direction.

5.3.2 Incremental movement operation mode (MOD: 51h)

Incremental movement is performed in synchronization with input of manual pulser signals in this operation mode.

The sign of RMV register will determine the operating direction.

At startup, the absolute value of RMV register is copied to RPLS register.

A command pulse is output in synchronization with the input of manual pulser signals, and RPLS register counts down. When “RPLS = 0”, the incremental movement stops and the operation mode ends.

When starting with setting “RMV = 0”, it ends without outputting the command pulse.

5.4 Switch control

It can be controlled by inputs of external switch signals (PDRn and MDRn).

With “PEn = L level”, input of external switch signal can be used.

By using PEn terminal, one set of external switches is changed to be used by multiple axes.

The input noise filter for PEn terminal and PDRn, MDRn terminal can be selected (RENV1.DRF).

When a start command is written, the operation status becomes “RSTS.CND = 0001b”.

After that, when an external switch signal is input to PDRn terminal or MDRn terminal, command pulses are output from OUTn terminal and DIRn terminal.

The external switch input terminals are shared with the manual pulser signal input terminals.

Input the positive side of external switch signal to PDRn terminal and the negative side to MDRn terminal.

The input logics of PDRn and MDRn terminals can be changed (RENV1.DRL).

The external switch signal can generate an event interrupt when the input changes.

The statuses of PDRn and MDRn terminals (RSTS.SPDR, RSTS.SMDR) can be read.

Sets the input logic of external switch signals (PDRn, MDRn) <RENV1.DRL(25)> 0: Negative logic 1: Positive logic	[RENV1] (R/W) 31 … 24 - - - - - - n -
Applies a noise filter (PEn, PDRn, MDRn) <RENV1.DRF(27)> 0: Recognizes signals with pulse width of 0.1 µs or wider. 1: Recognizes signals with pulse width of 54 ms or wider.	[RENV1] (R/W) 31 … 24 - - - - n - - -
Sets an event interrupt factor <RIRQ.IRDR(11)> 1: An interrupt is generated if the input to PDRn terminal or MDRn terminal changes. This interrupt also occurs in operation modes other than switch control.	[RIRQ] (R/W) 15 … 8 0 - - - n - - -
Obtains an event interrupt factor <RIST.ISMD(12), RIST.ISPD(11)> ISMD = 1: When the MDRn terminal input changes. ISPD = 1: When the PDRn terminal input changes.	[RIST] (R/W) 15 … 8 - - - n n - - -
Obtains an operation status <RSTS.CND(3 to0)> 0001b: Waiting for an external signal input	[RSTS] (R) 7 … 0 - - - - n n n n
Obtains the status of PDRn and MDRn terminals <RSTS.SMDR(12), RSTS.SPDR(11)> SMDR = 1: MDRn terminal is ON SPDR = 1: PDRn terminal is ON	[RSTS] (R) 15 … 8 - - - n n - - -

Remark: After starting, operation mode will not be terminated even if an alarm signal turns ON before operating with the input of external switch signal. Since an error interrupt is occurred, be sure to write STOP (49h) command and to exit the operation mode.

The external switch control has the following two operation modes:

MOD	Operation mode	Direction of movement
02h	Continuous movement	Determined by external switch signal input.
56h	Incremental movement	Determined by external switch signal input.

5.4.1 Continuous movement operation mode (MOD: 02h)

It is an operation mode to move continuously while the external switch signal is ON.

The operation mode can be terminated by writing STOP (49h) command.

The operating direction is the positive when PDRn terminal is ON and is the negative when MDRn terminal is ON. Although it stops when an end limit signal in the operating direction is ON, it can operate in the reverse direction without re-writing a start command. When an end limit signal in the operating direction is ON and stopped, no error interrupt is generated.

For STAD (52h) command or STAUD (53h) command, it decelerates and stops when an external switch signal turns OFF. If an external switch signal in the reverse direction turns ON while the external switch signal is OFF and decelerating, it can restart in the reverse direction after decelerating and stopping.

[Setting procedures]

1. Sets environment setting registers.
   Sets the operation mode of switch control continuous movement (PRMD.MOD = 02h).
2. Sets speed control registers.
3. Writes STAFL (50h), STAFH (51h), STAD (52h) or STAUD (53h) commands.
4. Waits for input of external switch signal (RSTS.CND = 0001b).
5. Inputs “PE = L level”.

When an external switch signal turns ON in this state, it operates in the specified direction at the speed pattern of start command.

5.4.2 Incremental movement operation mode (MOD: 56h)

It is an operation mode that performs an incremental movement by the change of external switch signal from OFF to ON. The operation mode can be terminated by writing STOP (49h) command.

Operation direction is positive if the switch signal on the positive side is ON, while it is negative if the switch signal on the negative side is ON.

Although the operation stops when the end limit signal in the operating direction turns ON, it can restart and operate in the reverse direction without writing the start command again. When the end limit signal in the operation direction turns ON and the operation stops, no error interrupt occurs.

While stopping, the absolute value of RMV register is copied to RPLS register when the external switch signal is changed from OFF to ON. After that, the command pulse starts to be output, and RPLS register starts to count down. Even if the external switch signal repeats OFF or ON during operation, it ignores the input and stops when “RPLS = 0”. You can continue to operate without writing a start command again.

When “RMV = 0”, pulses are not output by input of external switch signal, but the direction signal changes.

5.5 Origin return control

An operation starts by writing the start command.

A movement stops by inputting origin signal or encoder Z-phase signal and ends the operation mode.

Origin return control uses origin signals or encoder Z-phase signals depending on the operation mode. Input logic (RENV1.ORGL) and input noise filter (RENV1.FLTR) can be set to ORGn terminal to which the origin signal is input. The status of ORGn terminal (SSTS.SORG) can also be read.

To EZn terminal to input encoder Z-phase signal, you can set the input specifications (RENV2.EZL), specified number of times (RENV2.EZD) and input noise filter (RENV2.EINF).

The state of EZn terminal (RSTS.SEZ) can also be read.

In addition to latching and clearing the counter (RENV3) at the completion of an origin return control, the deviation counter clear signal output (RENV1.EROR) can be set.

For details on latching and clearing counters, see “7.1 Latch and clear (LTCn)”.

For details on the output of deviation counter clear signal, see “7.5.2 Deviation counter clear signal (ERCn)”.

Selects the input logic of ORG signal <RENV1.ORGL(7)> 0: Negative logic. 1: Positive logic.	[RENV1] (R/W) 7 0 n - - - - - - -
Input noise filter (PELn, MELn, SDn, ORGn, ALMn, INPn, CEMG) <RENV1.FLTR(26)> 0: Recognizes signals with pulse width of 0.1 μs or wider. 1: Recognizes signals whose pulse width is equal to or larger than the set value with RENV1.FTM bit.	[RENV1] (R/W) 31 24 - - - - - n - -
Input noise filter characteristics (PELn, MELn, SDn, ORGn, ALMn, INPn, CEMG) <RENV1.FTM(21, 20)> Selects the input noise filter characteristic of “RENV1.FLTR = 1” 00b : 3.2 μs 01b : 25 μs 10b : 200 μs 11b : 1.6 ms	[RENV1] (R/W) 23 16 - - n n - - - -
Reading ORGn terminal state <SSTS.SORG(14)> 0: ORGn terminal is OFF. 1: ORGn terminal is ON.	[SSTS] (R) 15 8 - n - - - - - -
Encoder Z-phase signal in origin return control. <RENV2.ORM(29)> 0: Not use encoder Z-phase signal. 1: Use encoder Z-phase signal.	[RENV2] (R/W) 31 24 - - n - - - - -
Input specification of encoder Z-phase signal <RENV2.EZL(28)> 0: Falling edge. 1: Rising edge.	[RENV2] (R/W) 31 24 - - - n - - - -

Input noise filter (EAn, EBn, EZn) <RENV2.EINF(18)> 0: Recognizes signals with pulse width of 0.1 µs or wider. 1: Recognizes signals with pulse width of 0.15 µs or wider.	[RENV2] (R/W) 23 16 - - - - - n - -
Set a specified number of encoder Z-phase count <RENV2 EZD(27 to 24)> The setting range is 0000b (first) to 1111b (16th).	[RENV2] (R/W) 31 24 - - - - n n n n
Reads encoder Z-phase counter <RSPD.EZC(19 to 18)> Input count value of encoder Z-phase signal used for origin return control can be read. It is a down counter and shows RENV2.EZD bit value when operation is stopped.	[RSPD] (R) 23 16 0 0 0 0 n n n n
Status of EZn terminal <RSTS.SEZ(10)> 1: When “RENV2.EZL = 0”, “EZn = L level”. When “RENV2.EZL = 1”, “EZn = H level”.	[RSTS] (R) 15 8 - - - - - n - -

Origin return control has 16 operation modes with combination of RMD.MOD bit, RENV2.ORM bit and start command.

When the output pulse mode is the common pulse mode or 2-pulse mode, the direction signal changes at the time of writing RMD register.

MOD	ORM	COMB0	Operation description
	0	50h	1. Constant speed operation at FL speed in positive direction. 2. Operation stops when origin signal turns from OFF to ON.
		51h	1. Constant speed operation at FH speed in positive direction. 2. Operation stops when origin signal turns from OFF to ON.
		52h	1. Constant speed operation at FH speed in positive direction. 2. Deceleration starts when origin signal turns from OFF to ON. When slow-down signal is ON and deceleration has been completed to FL speed, the operation stops. When deceleration to FL speed is completed, operation stops.
		53h	1. Accelerates from FL speed to FH speed in positive direction. 2. Deceleration starts when origin signal turns from OFF to ON. When slow-down signal is ON and deceleration has been completed to FL speed, the operation stops. 3. When deceleration to FL speed is completed, operation stops.
	1	50h	1. Constant speed operation at FL speed in positive direction. 2. After the origin signal turns from OFF to ON, the operation stops at the input of the specified number of encoder Z-phase signals.
		51h	1. Constant speed operation at FH speed in positive direction. After the origin signal turns from OFF to ON, the operation stops at the input of the specified number of encoder Z-phase signals.
		52h	1. Constant speed operation at FH speed in positive direction. 2. Deceleration starts when origin signal turns from OFF to ON. When slow-down signal is ON and deceleration has been completed to FL speed, the constant speed operation will continue at FL speed. 3. Operation stops when the specified number of encoder Z-phase signals is input. At this time, even if deceleration to FL speed has not been completed, it stops immediately.
		53h	1. Starts to accelerate from FL speed to FH speed in positive direction. 2. Starts to decelerate when origin input changes from OFF to ON. When slow-down signal is ON and deceleration has been completed to FL speed, the constant speed operation will continue at the FL speed. 3. Operation stops when the specified number of encoder Z-phase signals is input. At this time, even if deceleration to FL speed has not been completed, it stops immediately.

18h	0	50h	1. Constant speed operation at FL speed in negative direction. 2. Operation stops when the origin signal turns from OFF to ON.
		51h	1. Constant speed operation at FH speed in negative direction. 2. Operation stops when origin signal turns from OFF to ON.
		52h	1. Constant speed operation at FH speed in negative direction. 2. Starts to decelerate when the origin signal turns from OFF to ON. When slow-down signal is ON and deceleration has been completed to FL speed, the operation stops. 3. When deceleration to FL speed is completed, the operation stops.
		53h	1. Accelerate from FL speed to FH speed in negative direction. 2. Starts to decelerate when the origin signal turns from OFF to ON. When slow-down signal is ON and deceleration has been completed to FL speed, the operation stops. 3. When deceleration to FL speed is completed, the operation stops.
	1	50h	1. Constant speed operation at FL speed in negative direction. 2. Operation stops at the input of the specified number of encoder Z-phase signals after origin signal has turned from OFF to ON.
		51h	1. Constant speed operation at FH speed in negative direction. 2. Operation stops at the input of the specified number of encoder Z-phase signals after origin signal has turned from OFF to ON.
		52h	1. Constant speed operation at FH speed in negative direction. 2. Deceleration starts when origin signal turns from OFF to ON. When slow-down signal is ON and deceleration has been completed to FL speed, the constant speed operation will continue at FL speed. 3. Operation stops when the specified number of encoder Z-phase signals is input. Even if deceleration to FL speed has not been completed, operation stops immediately.
		53h	1. Accelerate from FL speed to FH speed in negative direction. 2. Deceleration starts when origin signal turns from OFF to ON. When slow-down signal is ON and deceleration has been completed to the speed, the constant speed operation will continue at FL speed. 3. Operation stops when the specified number of encoder Z-phase signals is input. Even if deceleration to FL speed has not been completed, operation stops immediately.

5.5.1 Origin return 0 operation mode (RENV2.ORM = 0)

An operation mode to perform origin return controls without using encoder Z- phase signal.

An example operation in the operation mode of positive direction origin return (RMD.MOD = 10h) is shown as follows:

△: Timing to output ON signal from ERCn terminal when “RENV1.EROR = 1” and the operation is completed.

▲: Timing to output ON signal from ERCn terminal when “RENV1.EROE = 1” and stopped by error. It is not output at FL speed.

↑: Timing to latch COUNTER 1 with “RENV3.CU1R=1” or to latch COUNTER 2 with “RENV3.CU2R=1”.

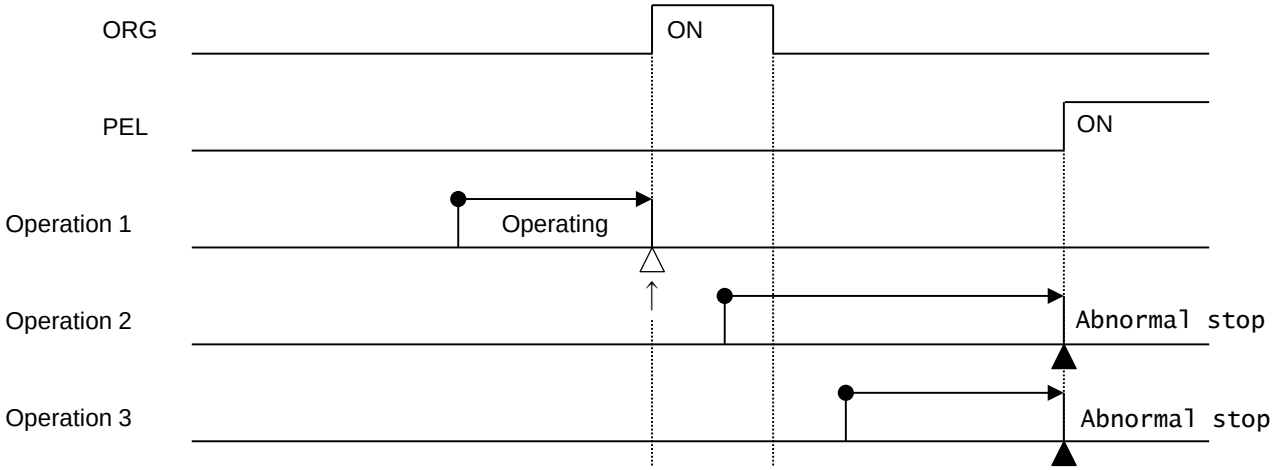
5.5.1.1 STAFH(51h) command

When “RENV1.EROR = 1” is set, ON can be output from ERCn terminal at the completion of operation.

When “RENV1.EROE = 1” is set, ON can be output from ERCn terminal at abnormal stop.

When “RENV3.CU1R = 1” and “RENV3.CU1L = 1” are set, Counter 1 can be cleared at the origin position.

When “RENV3.CU2R = 1” and “RENV3.CU2L = 1”, are set, Counter 2 can be cleared at the origin position.



5.5.1.2 STAFH(53h) command , immediate stop (RENV1.ELM=0)

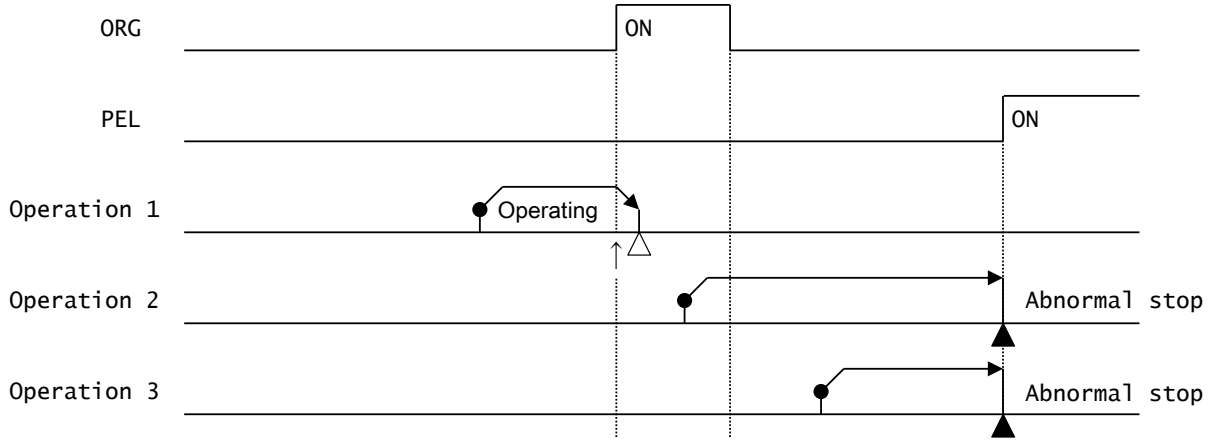
When the operation is completed, the origin position has already been passed. However, the counter value will be reliable.

When “RENV1.EROR = 1” is set, ON can be output from ERCn terminal at the completion of operation.

When “RENV1.EROE = 1” is set, ON can be output from ERCn terminal at abnormal stop.

When “RENV3.CU1R = 1” and “RENV3.CU1L = 1” are set, Counter 1 can be cleared at origin position.

When “RENV3.CU2R = 1” and “RENV3.CU2L = 1” are set, Counter 2 can be cleared at origin position.



5.5.1.3 STAUD(53h) command, Deceleration stops (RENV1.ELM=1)

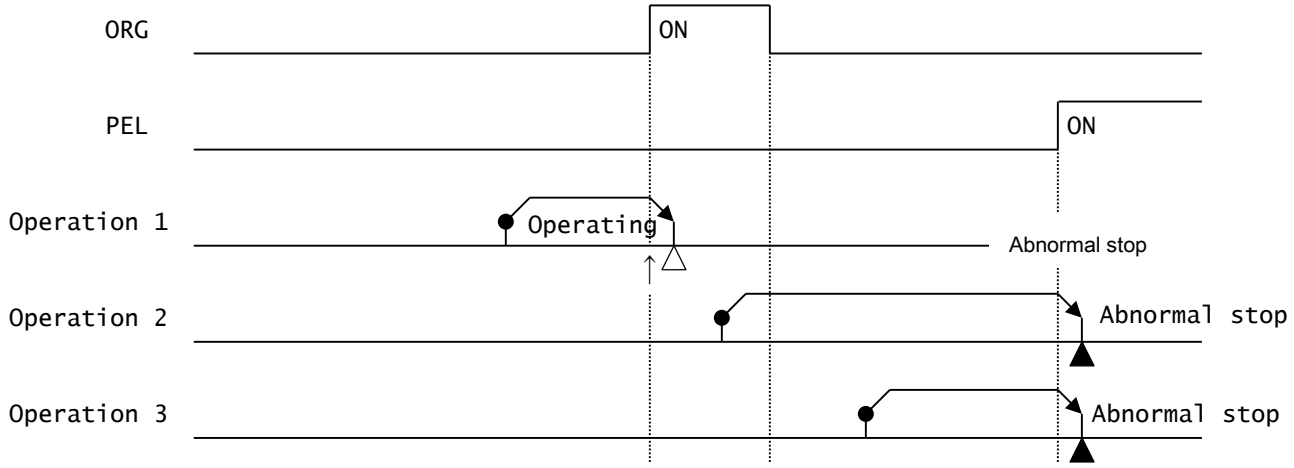
When the operation is completed, the origin position has already been passed. However the counter value will be reliable.

When “RENV1.EROR = 1” is set, ON can be output from ERCn terminal at the completion of operation.

When “RENV1.EROE = 1” is set, ON can be output from ERCn terminal at abnormal stop. It is not output when it reaches FL speed.

When “RENV3.CU1R = 1” and “RENV3.CU1L = 1” are set, Counter 1 can be cleared at origin position.

When “RENV3.CU2R = 1” and “RENV3.CU2L = 1” are set, Counter 2 can be cleared at origin position.



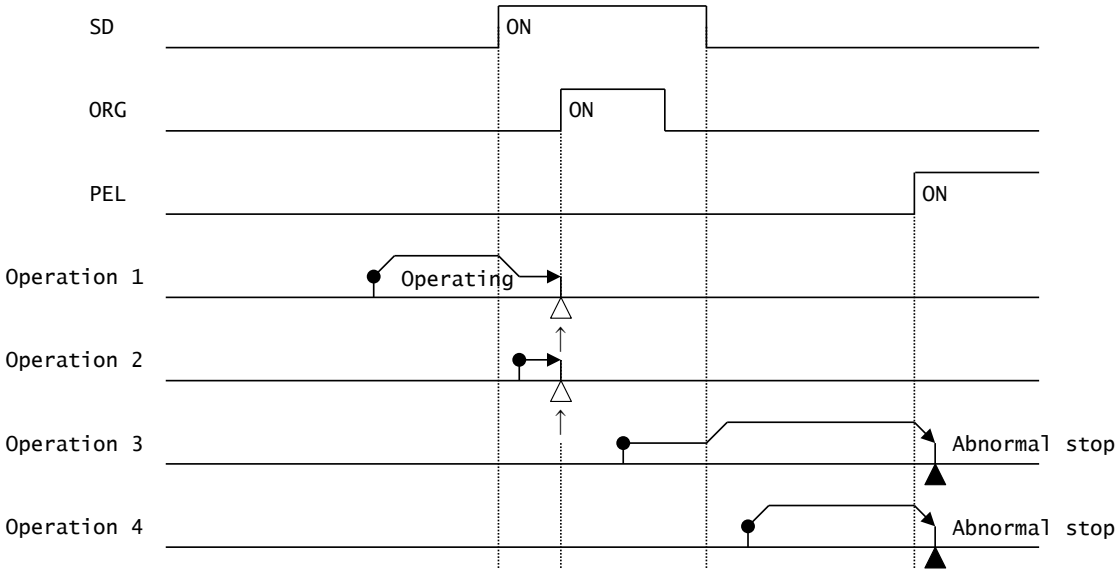
5.5.1.4 STAUD(53h) command, Deceleration stop(RENV1.ELM = 1), Deceleration (RENV1.SDM = 0), No SD latch(RENV1.SDLT = 0)

When “RENV1.EROR = 1” is set, ON can be output from ERCn terminal at the completion of operation.

When “RENV1.EROE = 1” is set, ON can be output from ERCn terminal at abnormal stop. It is not output when it reaches FL speed.

When “RENV3.CU1R = 1” and “RENV3.CU1L = 1” are set, Counter 1 can be cleared at origin position.

When “RENV3.CU2R = 1” and “RENV3.CU2L = 1” are set, Counter 2 can be cleared at origin position.



5.5.2 Origin return 1 operation mode (RENV2.ORM = 1)

An operation mode to perform origin return controls with encoder Z- phase signal.

An example operation of two times EZ count (RENV2.EZD = 0001b) in the operation mode of positive direction origin return (RMD.MOD = 10h) is shown as follows:

△: Timing to output ON signal from ERCn terminal when “RENV1.EROR = 1” and the operation is completed.

▲: Timing to output ON signal from ERCn terminal when “RENV1.EROE = 1” and stopped by error. It is not output at FL speed.

↑: Timing to latch COUNTER 1 with “RENV3.CU1R=1” or to latch COUNTER 2 with “RENV3.CU2R=1”.

5.5.2.1 STAFH(51h) command

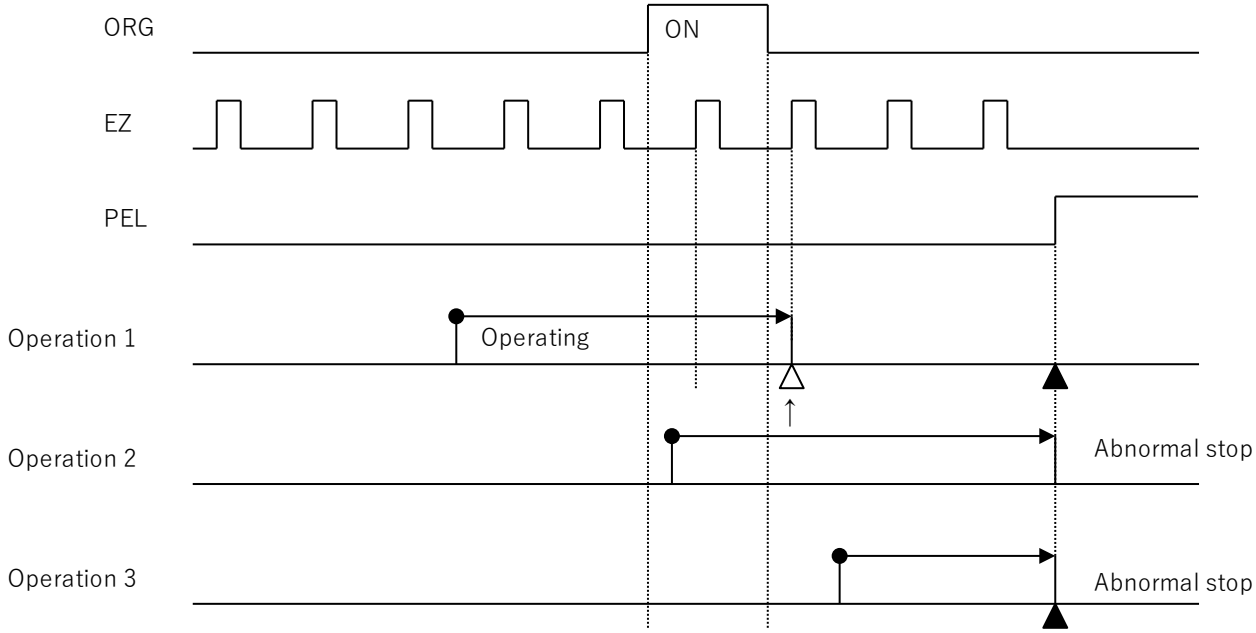
When “RENV1.EROR = 1” is set, ON can be output from ERCn terminal at the completion of operation mode.

The operation mode is completed when EZ count stops.

When “RENV1.EROE = 1” is set, ON can be output from ERCn terminal at abnormal stop.

When “RENV3.CU1R = 1” and “RENV3.CU1L = 1” are set, Counter 1 can be cleared at origin position.

When “RENV3.CU2R = 1” and “RENV3.CU2L = 1” are set, Counter 2 can be cleared at origin position.



5.5.2.2 STAUD(53h) command, Immediate stop (RENV1.ELM=0)

When “RENV1.EROR = 1” is set, ON can be output from ERCn terminal at the completion of operation.

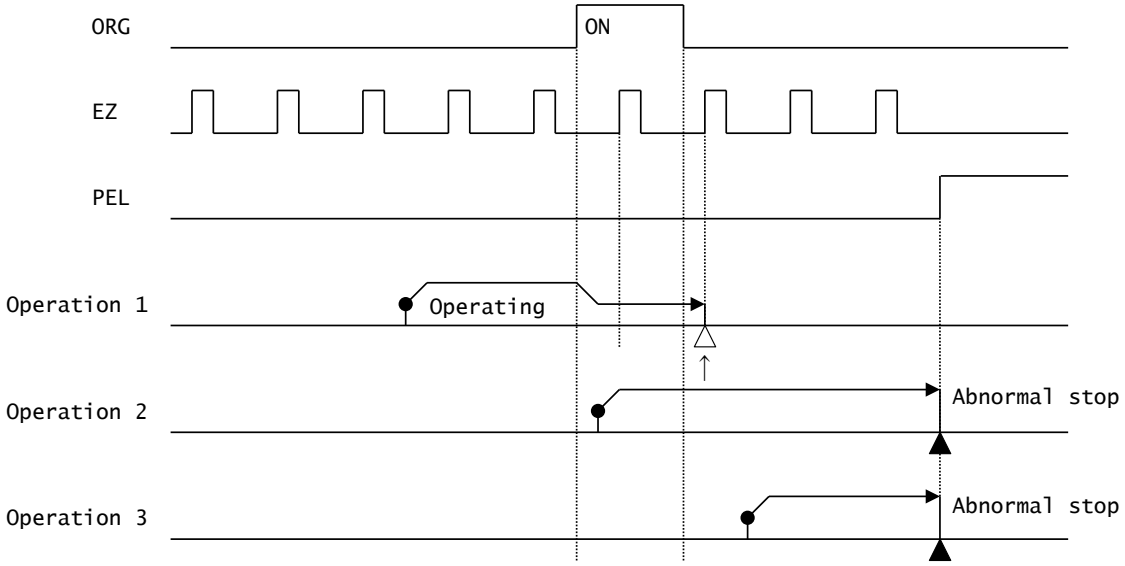
The operation is completed when EZ count stops.

When “RENV1.EROE = 1” is set, ON can be output from ERCn terminal at abnormal stop.

When “RENV3.CU1R = 1” and “RENV3.CU1L = 1” are set, Counter 1 can be cleared at origin position.

When “RENV3.CU2R = 1” and “RENV3.CU2L = 1” are set, Counter 2 can be cleared at origin position.

When EZ count is stopped during deceleration, an event interrupt factor (RIST.ISEZ) can be generated.



5.5.2.3 STAUD(53h) command, Deceleration stop (RENV1.ELM=1)

When “RENV1.EROR = 1” is set, ON can be output from ERCn terminal at the completion of operation.

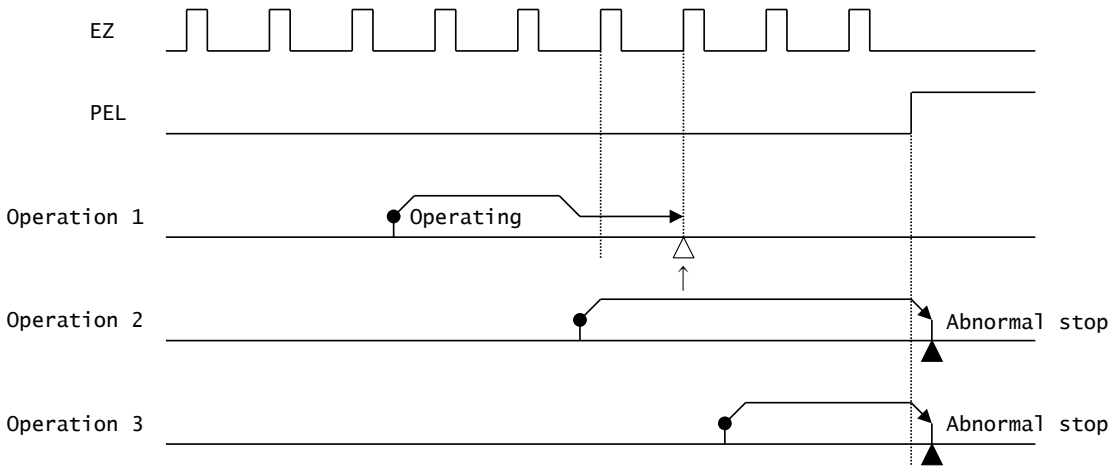
The operation is completed when EZ count stops.

When “RENV1.EROE = 1” is set, ON can be output from ERCn terminal at abnormal stop. It is not output when it reaches FL speed.

When “RENV3.CU1R = 1” and “RENV3.CU1L = 1” are set, Counter 1 can be cleared at origin position.

When “RENV3.CU2R = 1” and “RENV3.CU2L = 1” are set, Counter 2 can be cleared at origin position.

An event interrupt factor (RIST.ISEZ) can be generated when EZ count stops during deceleration by an origin signal.



5.5.2.4 STAUD(53h) command, Deceleration stop(RENV1.ELM = 1), Deceleration (RENV1.SDM = 0), No SD latch(RENV1.SDLT = 0)

When “RENV1.EROR = 1” is set, ON can be output from ERCn terminal at the completion of operation.

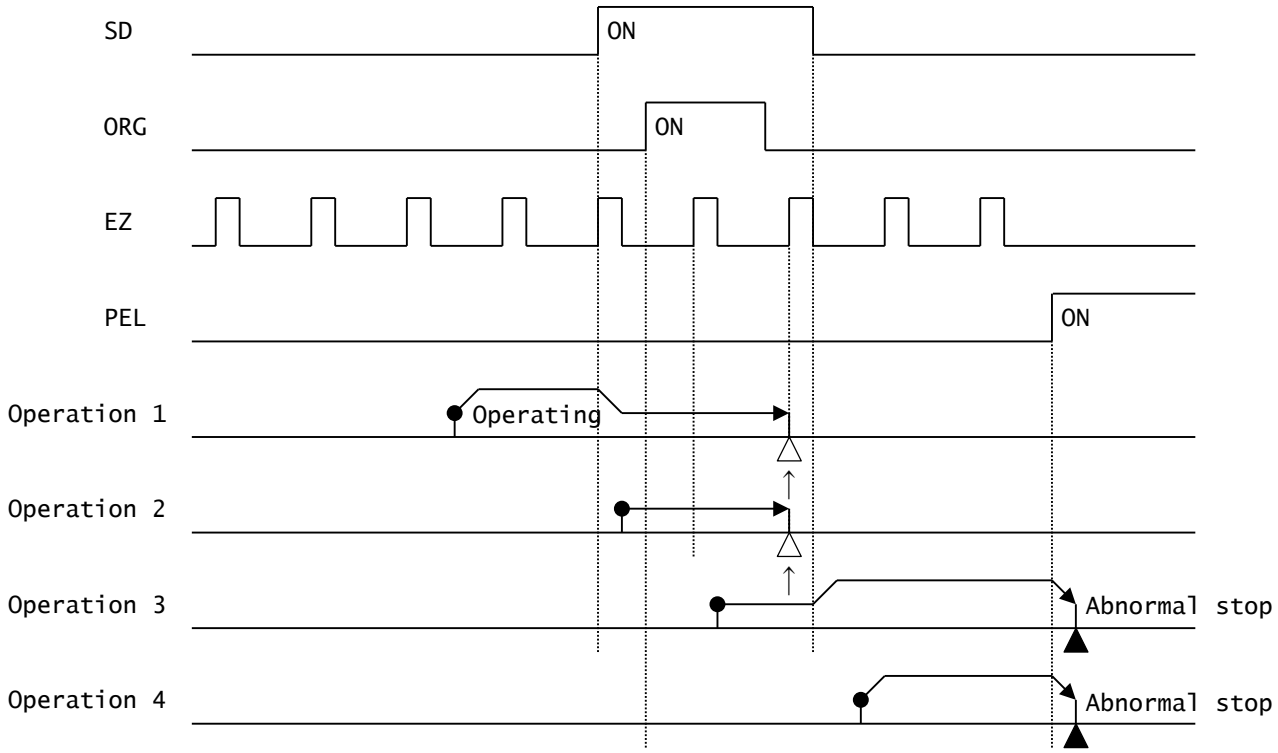
The operation is completed when EZ count stops.

When “RENV1.EROE = 1” is set, ON can be output from ERCn terminal at abnormal stop. It is not output when it reaches FL speed.

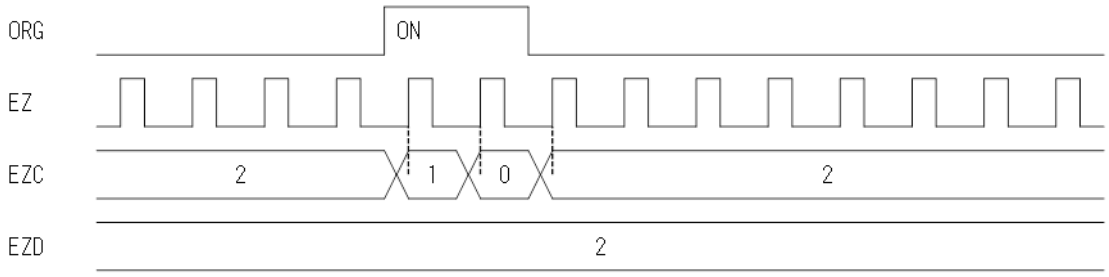
When “RENV3.CU1R = 1” and “RENV3.CU1L = 1” are set, Counter 1 can be cleared at origin position.

When “RENV3.CU2R = 1” and “RENV3.CU2L = 1” are set, Counter 2 can be cleared at origin position.

An event interrupt factor (RIST.ISEZ) can be generated when EZ count stops during deceleration by slow-down signal.



Remark: EZ count value can be read with RSPD.EZC. The default value of RSPD.EZC is the set value of RENV2.EZD. After origin signal turns ON, RSPD.EZC stops when encoder Z-phase signal counts down and returns the set value to RENV2.EZD following “0”.

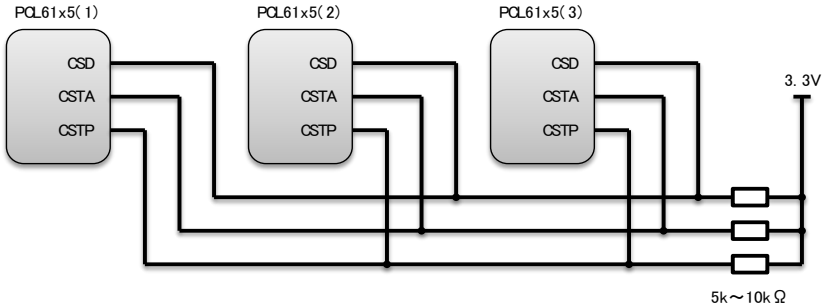


5.6 Linear interpolation control

Linear interpolation operation is performed on multiple axes in synchronization with the interpolation axis that has the largest feeding amount.

The linear interpolation circuit performs an interpolation between the dummy axis on each axis and its own-axis. Set the interpolation axis data with the largest feeding amount on all dummy axes and perform linear interpolations on all axes indirectly.

The interpolation axis operates independently, so it is necessary to start, decelerate, and perform an abnormal stop at the same time by an external signal. Therefore, even when using just a single LSI, make sure to pull-up (5 k to 10 kΩ) CSD, CSTA and CSTP terminals to VDD (3.3 V). When using multiple LSIs, connect CSD, CSTA, and CSTP terminals as shown below.



See “7.6 Simultaneous start” and “7.8 Simultaneous stop” for details.

Axes that are not involved in interpolation operations can operate independently. For example, PCL6145 can command control U-axis during linear interpolation control of X, Y, and Z axes.

There are two types of operation mode in linear interpolation control:

MOD	Operation mode	Operating direction
62h	Continuous movement	Positive direction when RMV≧0 Negative direction when RMV＜0
63h	Incremental movement	Positive direction when RMV≧0 Negative directing when RMV＜0

5.6.1 Continuous movement operation mode (MOD: 62h)

An operation mode to perform a continuous movement in accordance with the ratio of feeding amount set to the interpolation axis. The operation mode can be terminated by writing a stop command.

(Setting procedures)

1. Set “PRMD.MCDE = 1” and “PRMD.MCDO = 1” for all interpolation axes. Simultaneous slow-down can be performed when STAD (52h) command or STAUD (53h) command is used.
2. Set “PRMD.MSPE = 1” and “PRMD.MSPO = 1” for all interpolation axes.
   When any interpolation axis abnormally stops, all interpolation axes can be stopped at the same time.
3. Set signed feeding amounts to the PRMV registers of all interpolation axes.
   The sign specifies the direction of motion.

4. Set PRMV register absolute value of the axis whose feeding amount is the largest in the PRIP register of each axis.
5. Set the values of the speed control registers (PRFL, PRFH, PRUR, PRDR, PRMG, PRDP, PRUS, and PRDS) of the axes with the largest feeding amount, to each axis.

   When setting the synthesized speed, calculate the velocity component of the axis whose feeding amount is largest, and set it to each axis.

   For example, if the synthesized speed of two orthogonal axes is 5000 pps, the velocity component will be 4000 pps and 3000 pps. Therefore, set each speed control register value to 4000 pps, and set the ratio (PRMV) of 4 and 3.
6. When performing interpolations with a single LSI, you can specify the interpolation axis with the axis selection code when writing the start command. All interpolation axes start simultaneously. When performing interpolations with multiple LSIs, set “simultaneous start signal input wait (PRMD.MSY = 01b)” on all interpolation axes.

   Writing start command to all interpolation axes and waiting for simultaneous start signal input (RSTS.CND = 0010b).

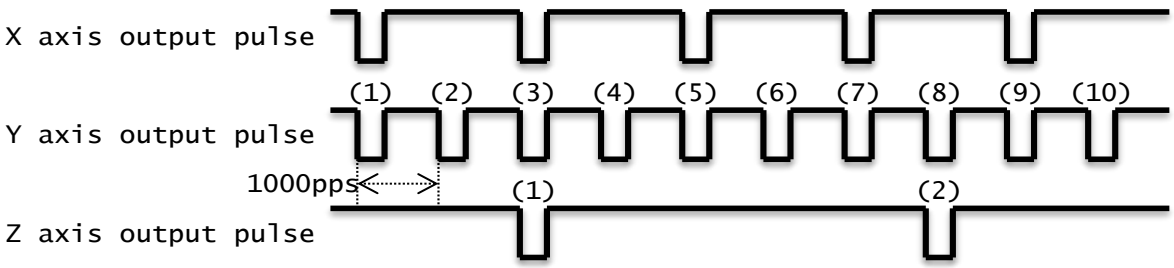
   If you write CMSTA (06h) command to any axis, all interpolation axes start simultaneously.
7. When performing interpolations with a single LSI, you can specify the interpolation axis with axis selection code when writing stop commands. All interpolation axes stop simultaneously. When performing interpolations with multiple LSIs, write CMSTP (07h) command to any axis. All axes stop simultaneously. An error interrupt occurs when simultaneous stop signal turns ON, so clear it. If “RENV2.CSPO = 1” is set, simultaneous stop signal can also be turned ON with STOP (49h) command.

[Setting example]

With PCL6145, if STAFH (0751h) command is written per the following setting, the command pulse is output as shown in the following operation example.

Setting target	X-axis	Y-axis	Z-axis	Explanation
PRMD.MOD	63h	63h	63h	Selects the operation mode of linear interpolation continuous movement.
PRMD.MSPE	1	1	1	Simultaneously stops by writing CMSTP (07h) command or inputting simultaneous stop signal.
PRMD.MSPO	1	1	1	A simultaneous stop signal is output at abnormal stop.
PRMD.MSY	00b	00b	00b	Starts without waiting for simultaneous start signal input after writing the Start command. When “PRMD.MSY = 01b” is set, the simultaneous start signal input wait state is entered. It starts by writing CMSTA (06h) command or inputting simultaneous start signal.
PRMD.MCDE	1	1	1	Decelerates simultaneously by inputting simultaneous slow-down signal.
PRMD.MCDO	1	1	1	Outputs simultaneous slow-down signal while decelerating.
PRMV	5h	Ah	2h	Sets the feeding amount (ratio).
PRIP	Ah	Ah	Ah	Sets the feeding amount of the interpolation axis with the largest feeding amount (Y-axis in this case).
PRFL	1000	1000	1000	Sets the FL speed of the interpolation axis with the largest feeding amount (Y-axis in this case). In case of FH constant speed start operation, it can be the same as FH speed.
PRFH	1000	1000	1000	Sets the FH speed of the interpolation axis with the largest feeding amount (Y-axis in this case).
PRMG	4AFh	4AFh	4AFh	Sets the speed magnification rate of the interpolation axis with the largest feeding amount (Y-axis in this case).

[Operation example]

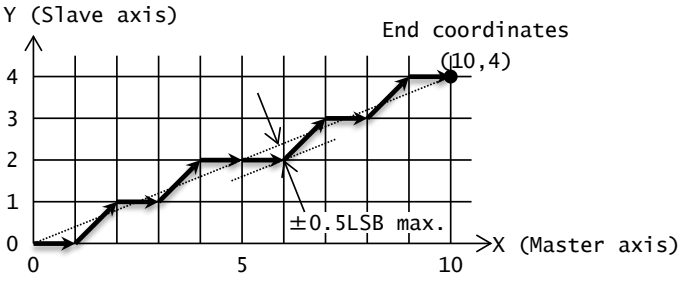


If the Y-axis is 1 (1000 pps), a linear interpolation operation is performed at the speed of 1/2 (500 pps) on X-axis and 1/5 (200 pps) on Z-axis.

[Precision of linear interpolation]

A linear interpolation is executed from the current coordinates to the end coordinates. The figure on the right shows an example straight line up to the end point coordinates of 10 and 4.

The position accuracy against the designated straight line during linear interpolation is ± 0.5 LSB within the entire interpolation section. The LSB is the minimum movement unit of RMV register value and is the interval between the squares in the right figure. It corresponds to the resolution of mechanical systems.



Remarks:

1. When acceleration/deceleration is performed using STAUD (53h) command, there are several restrictions as follows:
   (1) You need to set the same value for slow-down point setting method (PRMD.MSDP) and triangle drive avoidance (PRMD.MADJ) for all interpolation axes.
   (2) When selecting “PRMD.MSDP = 1” (manual setting) for slow-down point setting method, set the same value as the PRDP register value of interpolation axis with the largest feeding amount to all interpolaton axes.
2. For the interpolation axis set to “PRMD.MSPO = 1”, the simultaneous stop signal turns ON at an abnormal stop.
   If all the CSTP terminals are connected by pull-up connection, the interpolation axis set to “PRMD.MSPE = 1” also stops at the same time.
   The interpolated axis abnormally stopped is an interpolation axis that has not generateed the error interrupt factor “REST.ESSP = 1”. See “7.8 Simultaneous stop” for details.
3. For the interpolation axis set with “PRMD.MCDO = 1” and “PRMD.MSDE = 1” , simultaneous slow-down signal is ON when slow-down signal is ON.
   If all the CSD terminals are connected by pull-up connection, the interpolation axis set to “PRMD.MCDE = 1” will also decelerate at the same time. See “7.7 Simultaneous deceleration” for details.
4. By using pre-register, continuous linear interpolations can be performed, such as changing single axis operation or interpolated axis after an linear interpolation.
   For example, you can perform U-axis single operation after linear interpolation between X and Y axes, or continue linear interpolation between X and Z axes right after linear interpolation between X and Y axes.
   See “7.12.1 Starts by stopping the target axis” for details.

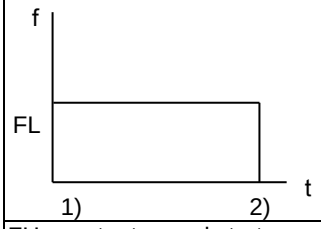
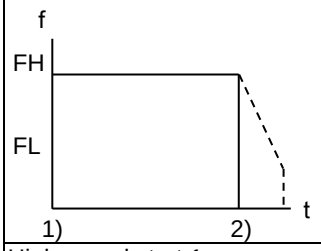
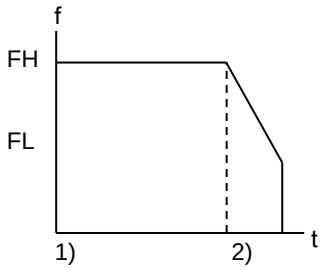
5.6.2 Incremental movement operation mode (MOD: 63h)

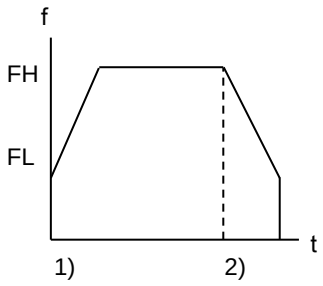
An operation mode to perform an incremental movement with the ratio of the feeding amount set to the interpolation axis.

The setting procedure, etc. is the same as the operation mode of continuous movement (MOD: 62h).

6. Speed controls

6.1 Speed pattern list

<table>
<tr><th>Speed pattern</th><th>Continuous movement operation mode</th><th>Incremental movement operation mode</th></tr>
<tr><td rowspan="2">FL constant speed start
 
</td><td>1) Write STAFL (50h) command.
2) Stop by writing STOP (49h) command or SDSTP (4Ah) command.</td><td>1) Write STAFL (50h) command.
2) Stop feeding by RPLS = “0” (positioning is completed), or by writing STOP (49h) command or SDSTP (4Ah) command.</td></tr>
<tr><td colspan="2">*FL constant speed pattern does not perform acceleration/deceleration operations by signal input to PELn, MELn, SDn, ALMn, CSTPn, ORGn, PDRn, or MDRn terminal.</td></tr>
<tr><td rowspan="2">FH constant speed start
 
</td><td>1) Write STAFH (51h) command.
2) Stop by writing STOP (49h) command.</td><td>1) Write STAFH (51h) command.
2) Stop feeding by RPLS = “0” (positioning is completed), or by writing STOP (49h) command.</td></tr>
<tr><td colspan="2">When SDSTP (4Ah) command is written, it will decelerate and stop.
FH constant speed pattern does not perform acceleration/deceleration operation by signal input to PELn, MELn, SDn, ALMn, CSTPn, ORGn, PDRn, or MDRn terminal.</td></tr>
<tr><td rowspan="2">High speed start 1
 
</td><td>1) Write STAD (52h) command.
2) Start to decelerate and stop by writing SDSTP (4Ah) command.

Stop immediately by writing STOP (49h) command.</td><td>1) Write STAD (52h) command.
2) Start decelerating and stop when a slow-down point is reached or by writing SDSTP (4Ah) command.
Immediately stops by writing “RPLS = 0” (positioning complete) or STOP (49h) command.
Automatic setting of slow-down point cannot be used.
Use “RMD.MSDP = 1” and set the appropriate value in RDP register.
If “RDP = 0”, deceleration is not performed, and stops immediately at “RPLS = 0” (positioning completes).</td></tr>
<tr><td colspan="2">In the speed pattern of high speed start 1, acceleration/deceleration is performed by signal input to PELn, MELn, SDn, ALMn, CSTPn, ORGn, PDRn or MDRn terminal.</td></tr>
<tr><td rowspan="2">High speed start 2
 
</td><td>1) Write STAUD (53h) command.
2) Start to decelerate and stop by writing SDSTP (4Ah) command.
Stop immediately by writing STOP (49h) command.</td><td>1) Write STAUD (53h) command.
2) Start decelerating and stop when a slow-down point is reached or by writing SDSTP (4Ah) command.
Immediately stops by writing “RPLS = 0” (positioning complete) or STOP (49h) command.
Automatic setting of slow-down point can be used.
Using “RMD.MSDP = 1”, if “RDP = 0”, it stops without deceleration, and stops immediately at “RPLS = 0” (positioning completes).</td></tr>
<tr><td colspan="2">In the speed pattern of High speed start 2, it accelerates/decelerates by signal input to PELn, MELn, SDn, ALMn, CSTPn, ORGn, PDRn, or MDRn terminal.</td></tr>
</table>

6.2 Speed pattern settings

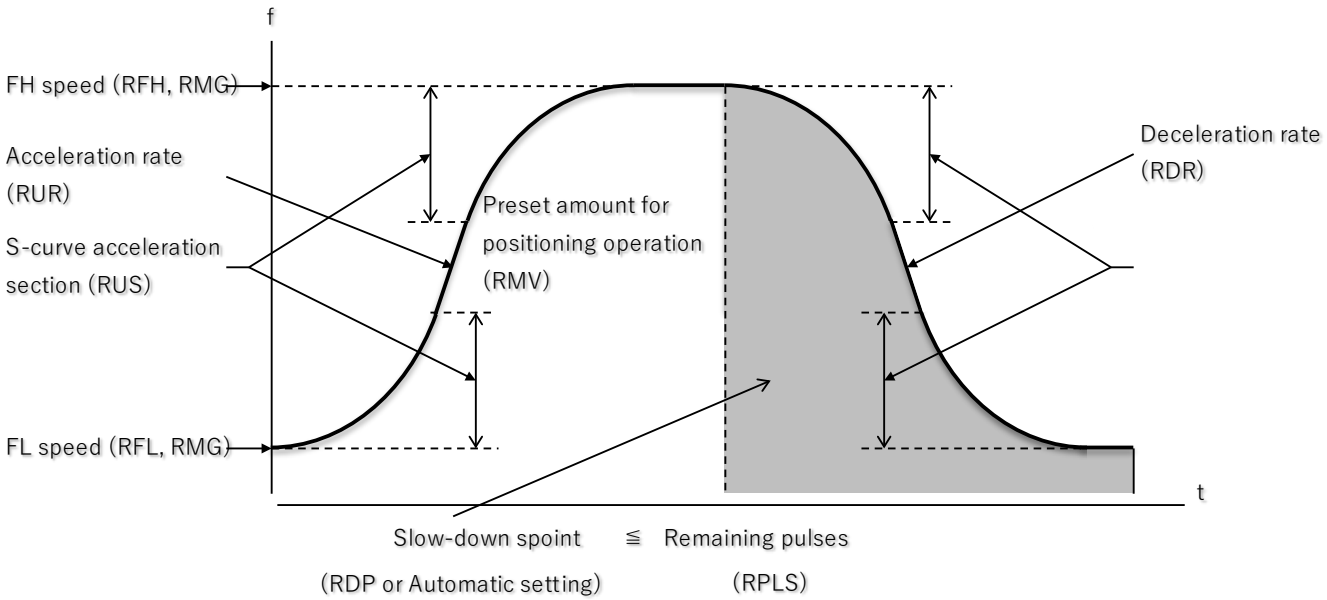
Speed setting is specified by using registers shown in the table below.

If the next setting value is the same as the current value, there is no need to write again.

No.	Name	Description	Length	Setting range			R/W
1.	RMV (PRMV)	Feeding '(Target position) amount setting	32	-2,147,483,648 (80000000h)	to	+2,147,483,647 (7FFFFFFFh)	R/W
2.	RFL (PRFL)	FL speed setting	14	1	to	16,383 (3FFFh)	R/W
3.	RFH (PRFH)	FH speed setting	14	1	to	16,383 (3FFFh)	R/W
4.	RUR (PRUR)	Acceleration rate setting	16	1	to	65,535 (FFFFh)	R/W
5.	RDR (PRDR)	Deceleration rate setting	16	0	to	65,535 (FFFFh)	R/W
6.	RMG (PRMG)	Speed magnification rate setting	12	1	to	4,095 (FFFh)	R/W
7.	RDP (PRDP)	Slow-down point setting	24	-8,388,608 (800000h)	to	+8,388,607 (7FFFFFh)	R/W
				0	to	16,777,215 (FFFFFFh)	
8.	RUS (PRUS)	S-curve acceleration section	13	0	to	8,191 (1FFFh)	R/W
9.	RDS (PRDS)	S-curve deceleration section	13	0	to	8,191 (1FFFh)	R/W

Note: When RDR = "0", the deceleration rate will be the value set in RUR register.

[Register setting data used for acceleration and deceleration]



Note: The time such as acceleration/deceleration calculated by the calculation formula, which will be described later, is an approximate value at the time of normal stop in continuous movement operation mode.

Approximation error is less than 1%. In incremental movement operation mode, the error can be 1% or more.

6.2.1 Speed control register calculation

6.2.1.1 RFL(PRFL): FL speed setting register

Sets the operation speed of FL constant speed start or sets the speed step to calculate the starting or stopping speed in high speed start 1 and 2.

FL speed is the calculated value with RMG register.

Calculate the relationship between FL speed and RFL register by the following formula.

$$\text{FL speed [pps]}=\text{RFL}\times\frac{\text{Reference clock frequency [Hz]}}{(\text{RMG}+1)\times 16384} \qquad \text{RFL}=\text{FL speed [pps]}\times\frac{(\text{RMG}+1)\times 16384}{\text{Reference clock frequency [Hz]}}$$

6.2.1.2 RFH(PRFH): FH speed setting register

Sets the operation speed of FH constant speed start or sets the speed step to calculate the operation speed in High speed start 1 and 2.

For high-speed start 1 and 2, set a larger value than of RFL register

FH speed is a calculated value with RMG register.

Calculate the relationship between FH speed and RFH register by the following formula.

$$\text{FH speed [pps]} = \text{RFH}\times\frac{\text{Reference clock frequency [Hz]}}{(\text{RMG}+1)\times 16384} \qquad \text{RFH}=\text{FH speed [pps]}\times\frac{(\text{RMG}+1)\times 16384}{\text{Reference clock frequency[Hz]}}$$

6.2.1.3 RUR(PRUR): Acceleration rate setting register

Sets the acceleration characteristics of high speed start 2.

Calculate the relationship between acceleration time and RUR register by the following formula.

1. Linear acceleration (RMD.MSMD = 0)

$$\text{Acceleration time[s]}=\frac{(\text{RFH}-\text{RFL})\times(\text{RUR}+1)\times 2}{\text{Reference clock frequency[Hz]}} \qquad \text{RUR}=\frac{\text{Reference clock frequency[Hz]}\times\text{Acceleration time[s]}}{(\text{RFH}-\text{RFL})\times 2}-1$$

2. Complete S-curve acceleration with no linear section (RMD.MSMD = 1, RUS = 0)

$$\text{Acceleration time[s]}=\frac{(\text{RFH}-\text{RFL})\times(\text{RUR}+1)\times 4}{\text{Reference clock frequency[Hz]}} \qquad \text{RUR}=\frac{\text{Reference clock frequency[Hz]}\times\text{Acceleration time[s]}}{(\text{RFH}-\text{RFL})\times 4}-1$$

3. Partial S-curve acceleration with linear section (RMD.MSMD = 1, RUS> 0)

$$\text{Acceleration time[s]}=\frac{(\text{RFH}-\text{RFL}+2\times\text{RUS})\times(\text{RUR}+1)\times 2}{\text{Reference clock frequency[Hz]}} \qquad \text{RUR}=\frac{\text{Reference clock frequency[Hz]}\times\text{Acceleration time[s]}}{(\text{RFH}-\text{RFL}+2\times\text{RUS})\times 2}-1-1$$

6.2.1.4 RDR(PRDR): Deceleration rate setting register

Sets the deceleration characteristics of high-speed start 2.

To select “RMD.MSDP = 0” (auto setting) for the slow-down point, set it the same as RUR register or set it to “0”.

When “RDR = 0” is set, the deceleration rate is shared with the RUR register.

Calculate the relationship between deceleration time and RDR register using the following formula.

1. Linear deceleration (RMD.MSMD = 0)

$$\text{Deceleration time [s]} = \frac{(\text{RFH} - \text{RFL}) \times (\text{RDR}+1) \times 2}{\text{Reference clock frequency [Hz]}} \qquad \text{RDR} = \frac{\text{Reference clock frequency [Hz]} \times \text{Deceleration time [s]}}{(\text{RFH} - \text{RFL}) \times 2} - 1$$

2. Complete S-curve deceleration with no linear section (“RMD.MSMD = 1”, “RDS = 0”)

$$\text{Deceleration time [s]} = \frac{(\text{RFH} - \text{RFL}) \times (\text{RDR}+1) \times 4}{\text{Reference clock frequency [Hz]}} \qquad \text{RDR} = \frac{\text{Reference clock frequency [Hz]} \times \text{Deceleration time [s]}}{(\text{RFH} - \text{RFL}) \times 4} - 1$$

3. Partial S-curve deceleration with linear section (“RMD.MSMD = 1”, “RUS > 0”)

$$\text{Deceleration time [s]} = \frac{(\text{RFH} - \text{RFL}+2\times\text{RDS}) \times (\text{RDR}+1) \times 2}{\text{Reference clock frequency [Hz]}} \qquad \text{RDR} = \frac{\text{Reference clock frequency [Hz]} \times \text{Deceleration time [s]}}{(\text{RFH} - \text{RFL}+2\times\text{RDS}) \times 2} - 1$$

6.2.1.5 RMG(PRMG): Speed magnification setting register

Sets the relationship between speed step and speed.

The higher the magnification is, the coarser the set speed interval becomes.

Be sure to use low magnification rate that meets the output speed range.

Calculate the relationship between speed magnification ratio and RMG register using the following formula.

$$\text{Magnification[Times]} = \frac{\text{Reference clock frequency [Hz]}}{(\text{RMG}+1) \times 16384} \qquad \text{RMG} = \frac{\text{Reference clock frequency [Hz]}}{\text{Magnification[Times]} \times 16384} - 1$$

[Examples of magnification rate setting when the reference clock frequency =19.6608 MHz]

Setting	Magnification rate	Output speed range[pps]	Setting	Magnification rate	Output speed range [pps]
3999 (0F9Fh)	0.3	0.3 to 4,914.9	59 (003Bh)	20	20 to 327,660
2399 (095Fh)	0.5	0.5 to 8,191.5	23 (0017h)	50	50 to 819,150
1199 (04AFh)	1	1 to 16.383	11 (000Bh)	100	100 to 1,638,300
599 (0257h)	2	2 to 32,766	5 (0005h)	200	200 to 3,276,600
239 (00EFh)	5	5 to 81,915	2 (0002h)	400	400 to 6,553,200
119 (0077h)	10	10 to 163,830	1 (0001h)	600	600 to 9,829,800

The maximum speed of this LSI can be output when the reference clock is 30 MHz, PRMG=“1”, and PRFH = “16383”.

At the time, the multiplication rate is 915.527× and the LSI outputs 14.999 Mpps.

6.2.1.6 RDP(PRDP): Slow-down point setting register

Sets slow-down point (deceleration start position).

The meaning(=role) of RDP register differs depending on the slow-down point setting method (RMD.MSDP).

<Automatic slow-down point setting (RMD.MSDP =0) >

Sets the offset of automatic slow-down point setting.

When the offset is a positive number, deceleration starts earlier, and it stops after operating at FL speed following completion of deceleration.

On the contrary, when it is a negative number, deceleration start is delayed and stops before reaching the FL speed.

Set “0” when offset is not necessary.

<Manual slow-down point setting (RMD.MSDP=1)>

Set the slow-down point directly.

When RPLS register (remaining pulse count) value becomes lower than RDP register value, a deceleration starts.

Note: To obtain the value of slow-down point manual setting, the value of operation speed is necessary. If the feeding amount is small, and deceleration is required during acceleration, or the operation speed is automatically corrected with the setting of “RMD.MADJ = 0” (triangle drive avoidance), the value of slow-down point manual setting cannot be calculated. If slow-down point setting method is “RMD.MSDP = 1” (manual setting), set to “RMD.MADJ = 1” (No triangle drive avoidance). In following calculations, the operation speed after manual FH correction calculation is used.
For details on calculation of operating speed which does not become triangular drive, see “6.3 Manual FH correction calculation”.

The optimum value of the slow-down point is calculated as follows.

1) Linear deceleration (RMD.MSMD=“0”)

$$\text{RDP [pulses]} = \frac{(PRFH^2 - PRFL^2) \times (RDR + 1)}{(RMG + 1) \times 16384}$$

2) Complete S-curve deceleration without a linear section (“RMD.MSMD = 1” and “RDS = 0”)

$$\text{RDP [pulses]} = \frac{(RFH^2 - RFL^2) \times (RDR + 1) \times 2}{(RMG + 1) \times 16384}$$

3) Partial S-curve deceleration with linear section (“RMD.MSMD = 1” and “RDS > 0”)

$$\text{RDP [pulses]} = \frac{(RFH + RFL) \times (RFH - RFL + 2 \times RDS) \times (RDR + 1)}{(RMG + 1) \times 16384}$$

If it is larger than the optimum value, deceleration starts earlier and stops after operating at FL speed after completing deceleration.

On the other hand, if it is less than the optimum value, the deceleration start is delayed and stops before reaching FL speed.

6.2.1.7 RUS(PRUS): Acceleration S-curve section setting register

Sets S-curve acceleration section in S-curve acceleration/deceleration operation.

The range of S-curve acceleration section S_{SU} is the calculated value with RMG register.

The relationship between S_{SU} and RUS register is calculated by the following formula.

$$S_{SU}[pps]=RUS\times\frac{\text{Reference clock frequency [Hz]}}{(RMG+1)\times16384} \qquad RUS=S_{SU}[pps]\times\frac{(RMG+1)\times16384}{\text{Reference clock frequency [Hz]}}$$

From FL speed to “FL speed + SSU” and “FH speed – SSU” to FH speed become partial S-curve acceleration operation, the middle section becomes linear acceleration operation. If the S-curve acceleration section is very short, such as setting S-curve acceleration section (SSU) to 1 pps or less, it will look to be a linear acceleration. When “0” is set, it becomes complete S-curve acceleration with no linear accelerating section using $\frac{RFH-RFL}{2}$.

6.2.1.8 RDS(PRDS): Deceleration S-curve section setting register

Sets S-curve deceleration section in S-curve acceleration/deceleration operation.

The range of S-curve deceleration section S_{SD} is the calculated value with RMG register.

The relationship between S_{SD} and RDS register is calculated by the following formula.

$$S_{SD}[pps]=RDS\times\frac{\text{Reference clock frequency [Hz]}}{(RMG+1)\times16384} \qquad RDS=S_{SD}[pps]\times\frac{(RMG+1)\times16384}{\text{Reference clock frequency [Hz]}}$$

From FH speed to “FH speed – S_{SD}” and “FL speed + S_{SD}” to FL speed become partial S-curve deceleration operation, the middle section becomes linear deceleration operation. If the S-curve deceleration section is very short, such as setting S-curve deceleration section (SSD) to 1 pps or less, it looks to be a linear deceleration. When “0” is set, it becomes complete S-curve deceleration with no linear deceleration section using $\frac{RFH-RFL}{2}$.

6.2.2 Speed pattern setting example

The following is an example;

Reference clock frequency = 19.6608 MHz, FL speed = 10 pps, FH speed = 100 kpps, Acceleration/deceleration time = 300 ms, Linear acceleration/deceleration.

1. FH speed is 100 kpps; set the magnification of 10 times, so that the actual speed range is 100 kpps or more.

   RMG = 119 (0077h)

2. The magnification is set to 10 times, so that FH speed to becomes 100 kpps,

   RFH = 10000 (2710h)

3. Tthe magnification is set to 10 times, in order to make FL speed to 10 pps, RFL=1(0001h)

   RFL = 1(0001h)

4. In order to make acceleration time to 300 ms, with the calculation of acceleration time and RUR register;

$$\mathrm{RUR} = \frac{\text{Reference clock frequency [Hz]} \times \text{acceleration time[s]}}{(\mathrm{RFH} - \mathrm{RFL}) \times 2} - 1$$
$$= \frac{19.6608 \times 10^6[\mathrm{Hz}] \times 0.3[\mathrm{s}]}{(10000 - 1) \times 2} - 1$$

$$\therefore \mathrm{RUR} = 293.94$$

Since the setting of RUR register is done only by an integer, set 293 or 294 to RUR register.

The acceleration time in this case is 299.04 ms (RUR = 293) or 300.06 ms (RUR = 294).

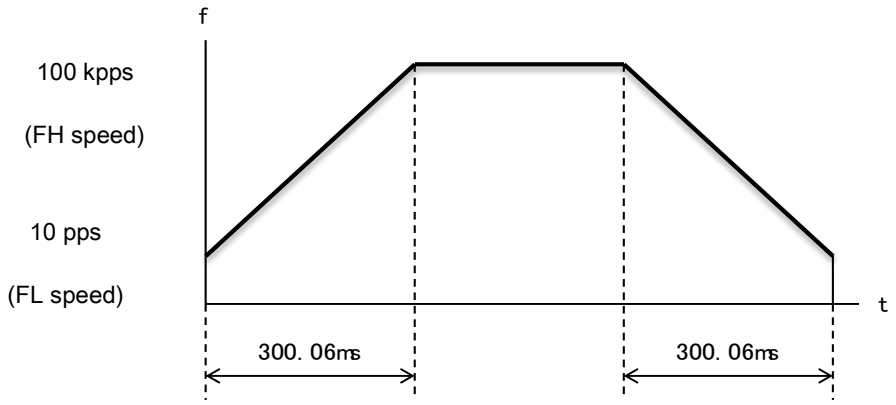
5. Since the acceleration time and the deceleration time are equal, set “0” to RDR register and share with RUR register.

<Example of speed setting when RUR = 294>

Note: Register names are used during calculation but be sure to use pre-register when writing.

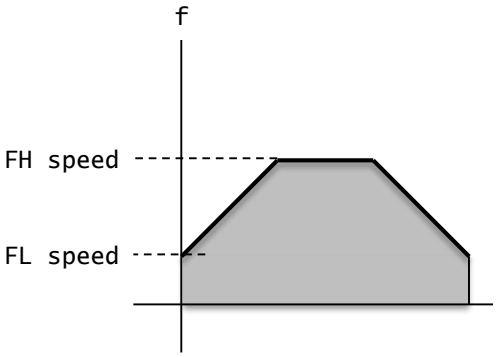
Name	Set value	Actual value
PRFL	1h	10 pps
PRFH	2710h	100 kpps
PRMG	77h	10 times
PRUR	126h	300.06 ms
PRDR	0h	RUR commonly used

<Example of speed pattern when RUR = 294>

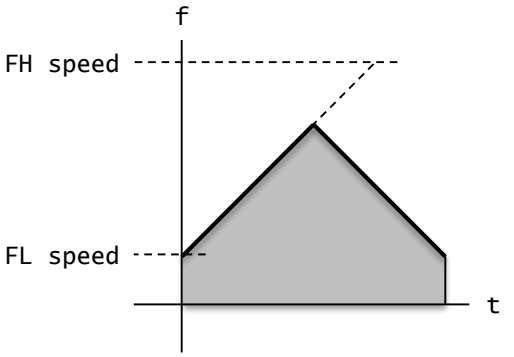


6.3 Manual FH correction calculation

When accelerating/decelerating in incremental movement operation mode, the speed pattern may become a triangle drive. If the FH speed is too high against the feeding amount, or if the feeding amount is too small against the FH speed, a triangle drive may occur.

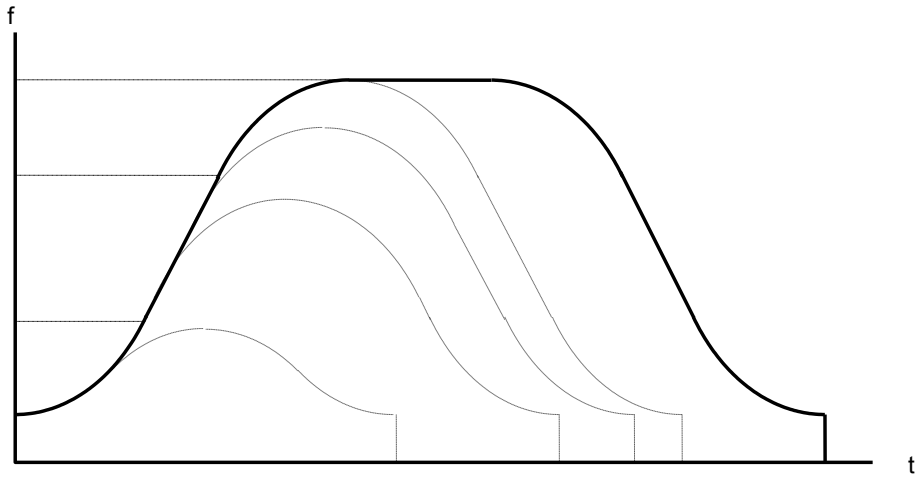


Normal linear acceleration /deceleration



Deceleration in the middle of acceleration
(Triangle drive)

When “RMD.MADJ = 0” (to avoid triangle drive), triangle drive is automatically avoided by lowering FH speed. If the slow-down point setting method is “RMD.MSDP = 0” (automatic setting), slow-down point is also corrected.



Automatic correction of operation speed in proportion to feeding amount.

The automatic setting of slow-down point can only be used when the acceleration curve and the deceleration curve are symmetrical. When the acceleration curve and the deceleration curve are not symmetric, select “PRMD.MSDP = 1” (manual setting) for slow-down point setting. See “6.2.1.6 RDP (PRDP): Slow-down point setting register” for details.

How to obtain the FH speed to avoid triangle drives when the acceleration curve and the deceleration curve are not symmetric, will be explained below:

Note: The result calculated by the formula described below is an approximate value. Approximate error is less than 1%.

6.3.1 Linear acceleration/deceleration speed

FH speed when “RMD.MSMD = 0” (linear acceleration/deceleration) is set, will be calculated by the following formula.

Condition: $$\mathrm{RMV} \leqq \frac{(\mathrm{RFH}^2 - \mathrm{RFL}^2) \times (\mathrm{RUR} + \mathrm{RDR} + 2)}{(\mathrm{RMG} + 1) \times 16384}$$ When

Result: $$\mathrm{RFH} \leqq \sqrt{\frac{(\mathrm{RMG} + 1) \times 16384 \times \mathrm{RMV}}{\mathrm{RUR} + \mathrm{RDR} + 2} + \mathrm{RFL}^2}$$

6.3.2 Complete S-curve acceleration/deceleration

FH speed in the case of setting “RMD.MSMD = 1”, “RUS = 0”, “RDS = 0” (complete S-curve acceleration/deceleration without linear acceleration/deceleration section) is calculated by the following formula.

Condition: $$\mathrm{RMV} \leqq \frac{(\mathrm{RFH}^2 - \mathrm{RFL}^2) \times (\mathrm{RUR} + \mathrm{RDR} + 2) \times 2}{(\mathrm{RMG} + 1) \times 16384}$$ When

Result: $$\mathrm{RFH} \leqq \sqrt{\frac{(\mathrm{RMG} + 1) \times 16384 \times \mathrm{RMV}}{(\mathrm{RUR} + \mathrm{RDR} + 2) \times 2} + \mathrm{RFL}^2}$$

6.3.3 Partial S-curve acceleration/deceleration

FH speed when partial S-curve acceleration/deceleration (RMD.MSMD = 1, RUS > 0 or RDS > 0) is set, will be calculated by the following formula for RUS register and RDS register.

Note: If the condition is not met, it is necessary to change RUS register and RDS register.

6.3.3.1 RUS = RDS

1. When the linear acceleration/deceleration section can be shorter:

Condition: $$\mathrm{RMV} \leqq \frac{(\mathrm{RFH} + \mathrm{RFL}) \times (\mathrm{RFH} - \mathrm{RFL} + 2 \times \mathrm{RUS}) \times (\mathrm{RUR} + \mathrm{RDR} + 2)}{(\mathrm{RMG} + 1) \times 16384}$$ And

$$\mathrm{RMV} > \frac{(\mathrm{RUS} + \mathrm{RFL}) \times \mathrm{RUS} \times (\mathrm{RUR} + \mathrm{RDR} + 2) \times 8}{(\mathrm{RMG} + 1) \times 16384}$$ When

Result: $$\mathrm{RFH} \leqq -\mathrm{RUS} + \sqrt{(\mathrm{RUS} - \mathrm{RFL})^2 + \frac{(\mathrm{RMG} + 1) \times 16384 \times \mathrm{RMV}}{(\mathrm{RUR} + \mathrm{RDR} + 2)}}$$

2. When the linear acceleration/deceleration sections can be eliminated.

Condition: $$\mathrm{RMV} \leqq \frac{(\mathrm{RUS} + \mathrm{RFL}) \times \mathrm{RUS} \times (\mathrm{RUR} + \mathrm{RDR} + 2) \times 8}{(\mathrm{RMG} + 1) \times 16384}$$ When

Change to complete S-curve acceleration/deceleration (RUS = 0, RDS = 0) without linear acceleration/deceleration section,

Result: $$\mathrm{RFH} \leqq \sqrt{\frac{(\mathrm{RMG} + 1) \times 16384 \times \mathrm{RMV}}{(\mathrm{RUR} + \mathrm{RDR} + 2) \times 2} + \mathrm{RFL}^2}$$

6.3.3.2 RUS<RDS

1. When the linear acceleration/deceleration section can be shorter:

Condition: $RMV \leqq \frac{(RFH + RFL) \times \{(RFH - RFL) \times (RUR + RDR + 2) + 2 \times RUS \times (RUR + 1) + 2 \times RDS \times (RDR + 1)\}}{(RMG + 1) \times 16384}$ And

$RMV > \frac{(RDS + RFL) \times \{RDS \times (RUR + 2 \times RDR + 3) + RUS \times (RUR + 1)\} \times 4}{(RMG + 1) \times 16384}$ When

Result: $RFH \leqq \frac{-A + \sqrt{A^2 + B}}{RUR + RDR + 2}$

However, $A = RUS \times (RUR + 1) + RDS \times (RDR + 1)$

$B = \{(RMG + 1) \times 16384 \times RMV - 2 \times A \times RFL + (RUR + RDR + 2) \times RFL^2\} \times (RUR + RDR + 2)$

2. When the linear acceleration section can be shorter, and the linear deceleration section can be removed:

Condition: $RMV \leqq \frac{(RDS + RFL) \times \{RDS \times (RUR + 2 \times RDR + 3) + RUS \times (RUR + 1)\} \times 4}{(RMG + 1) \times 16384}$ And

$RMV > \frac{(RUS + RFL) \times RUS \times (RUR + RDR + 2) \times 8}{(RMG + 1) \times 16384}$ When

Change to complete S-curve acceleration/deceleration without linear deceleration section (RUS> 0, RDS = 0),

Result: $RFH \leqq \frac{-A + \sqrt{A^2 + B}}{RUR + 2 \times RDR + 3}$

However, $A = RUS \times (RUR + 1)$

$B = \{(RMG + 1) \times 16384 \times RMV - 2 \times A \times RFL + (RUR + 2 \times RDR + 3) \times RFL^2\} \times (RUR + 2 \times RDR + 3)$

3. When the linear acceleration/deceleration section can be eliminated:

Condition: $RMV \leqq \frac{(RUS + RFL) \times RUS \times (RUR + RDR + 2) \times 8}{(RMG + 1) \times 16384}$ When

Change to complete S-curve acceleration/deceleration without linear accel/decel section (RUS= 0, RDS = 0),

Result: $RFH \leqq \sqrt{\frac{(RMG + 1) \times 16384 \times RMV}{(RUR + RDR + 2) \times 2} + RFL^2}$

6.3.3.3 When RUS>RDS

1. When the linear acceleration/deceleration section can be shorter:

Condition: $RMV \leqq \frac{(RFH + RFL) \times \{(RFH - RFL) \times (RUR + RDR + 2) + 2 \times RUS \times (RUR + 1) + 2 \times RDS \times (RDR + 1)\}}{(RMG + 1) \times 16384}$ And

$RMV > \frac{(RUS + RFL) \times \{RUS \times (2 \times RUR + RDR + 3) + RDS \times (RDR + 1)\} \times 4}{(RMG + 1) \times 16384}$ When

Result: $RFH \leqq \frac{-A + \sqrt{A^2 + B}}{RUR + RDR + 2}$

However, $A = RUS \times (RUR + 1) + RDS \times (RDR + 1)$

$B = \{(RMG + 1) \times 16384 \times RMV - 2 \times A \times RFL + (RUR + RDR + 2) \times RFL^2\} \times (RUR + RDR + 2)$

2. When linear deceleration section can be shorter and the linear acceleration section can be eliminated,

Condition: $RMV \leqq \frac{(RUS + RFL) \times \{RUS \times (2 \times RUR + RDR + 3) + RDS \times (RDR + 1)\} \times 4}{(RMG + 1) \times 16384}$ And

$RMV > \frac{(RDS + RFL) \times RDS \times (RUR + RDR + 2) \times 8}{(RMG + 1) \times 16384}$ When

Change to complete S-curve acceleration/deceleration (RUS = 0, RDS > 0) without linear acceleration section,

Result: $RFH \leqq \frac{-A + \sqrt{A^2 + B}}{2 \times RUR + RDR + 3}$

However, $A = RDS \times (RDR + 1)$

$B = \{(RMG + 1) \times 16384 \times RMV - 2 \times A \times RFL + (2 \times RUR + RDR + 3) \times RFL^2\} \times (2 \times RUR + RDR + 3)$

3. When the linear acceleration/deceleration section can be eliminated:

Condition: $RMV \leqq \frac{(RDS + RFL) \times RDS \times (RUR + RDR + 2) \times 8}{(RMG + 1) \times 16384}$ When

Change to complete S-curve acceleration/deceleration (RUS= 0, RDS = 0) without linear accel/decel section,

Result: $RFH \leqq \sqrt{\frac{(RMG + 1) \times 16384 \times RMV}{(RUR + RDR + 2) \times 2} + RFL^2}$

6.4 Target speed override

In the operation mode of command control continuous movement (RMD.MOD = 00h, 08h) and positioning control incremental movement (RMD.MOD = 41h), the target speed can be overridden by rewriting RFH register during operation. In the command control operation mode, the speed pattern can also be changed by rewriting RUR, RDR, RUS, and RDS registers during operation. If FH speed is automatically corrected by triangle drive avoidance function, FH speed cannot be changed even if RFH register is rewritten.

When slow-down point setting method is “RMD.MSDP = 0” (automatic setting) in positioning control incremental movement operation mode, there will be the following limitations;

If you do not follow these restrictions, slow-down point automatic setting function cannot be performed properly.

If deceleration start is delayed, it stops before reaching FL speed.

If deceleration starts earlier, it moves at FL speed after deceleration is completed.

[During linear acceleration/deceleration]

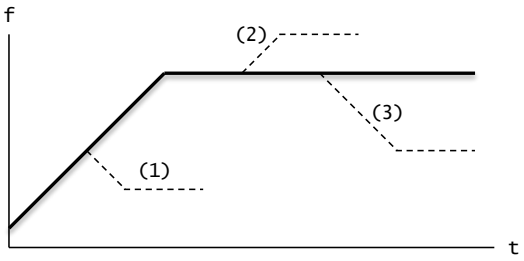
1. Since “RMD.MSDP = 0”, sets “RUR = RDR” or “RDR = 0”, to make acceleration/deceleration characteristic symmetrical.
2. Do not rewrite speed control registers other than RFH register during operation.

[During S-curve acceleration/deceleration]

1. Since “RMD.MSDP = 0”, sets “RUR = RDR”, or “RDR = 0”, to make acceleration/deceleration characteristic symmetrical.
2. Do not rewrite speed control registers other than RFH register during operation.
3. Do not change RFH register during acceleration or deceleration.
4. Set to “RMD.MADJ = 1” (no triangle drive avoidance).
5. If slow-down point is reached and deceleration is started during acceleration due to the speed change, it will stop before reaching to FL speed. Therefore, please pay attention to the timing to change the speed.

When slow-down point setting is “RMD.MSDP = 1” (manual setting), you can override the target speed and acceleration/deceleration speed at any time.

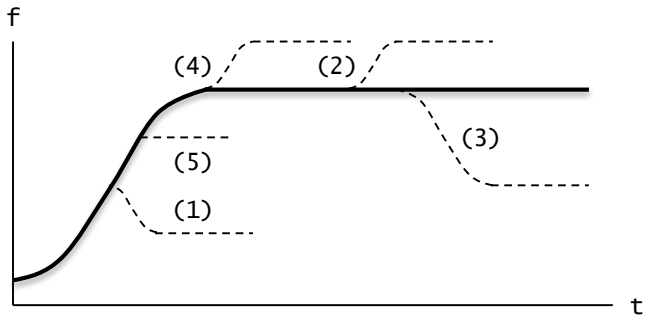
An example of changing the speed pattern by changing the speed during a linear acceleration/deceleration operation.



1) Rewrite RFH register while accelerating: If the changed speed is less than the current speed, it decelerates to that speed linearly.

2) 3) Change RFH register after acceleration is completed: Linearly accelerates or linearly decelerates to the speed.

Example of speed pattern change due to the speed change during S-curve acceleration/deceleration



1) Rewrite RFH register during acceleration: If the changed speed is less than the current speed, it decelerates with s-curve to that speed.

5) Rewrite RFH register during acceleration: If the changed speed is equal to or higher than the current speed and equal to or lower than the original target speed, it will accelerate without changing S-curve characteristic.

4) Rewrite RFH register during acceleration: If the changed speed exceeds the original target speed, accelerate to the original target speed without changing the S-curve characteristic and re-accelerates to that speed.

2), 3) Rewrite RFH register after acceleration is completed: S-curve acceleration or deceleration is performed to that speed.

7. Functions

7.1 Reset

After turning ON the power, make sure to reset the LSI at least once before beginning to use it.

To reset the LSI, input at least 8 cycles or more of reference clock signal while “RST = L level”.

The status after reset is configured as follows.

Item	Default status (Reset status)
Internal registers, pre-registers	0
Control command buffer	0
Axis assignment buffer	0
I/O buffer	0
INT terminal	H level
WRQ terminal	H level
IFB terminal	H level
D0 to D7 terminals	Parallel-bus interface: Hi-Z Serial-bus interface: Input terminal
D8 to D15 terminals	Parallel-bus interface: Hi-Z Serial-bus interface: Input terminal
P0n to P7n terminals	Input terminal
CSD terminal	H level
CSTA terminal	H level
CSTP terminal	H level
OUTn terminal	H level
DIRn terminal	H level
ERCn terminal	H level
BSYn terminal	H level

Note:

The internal status before resetting is unstable, and the terminal functions and output levels are not fixed.

From power ON to resetting, bi-directional terminals may be output terminals or L level signal may be output.

7.2 Target position override

Target position override can be performed during operation mode of incremental movement with positioning control (RMD.MOD = 41h). Do not override target positions in other operation modes.

There are two ways to override target positions.

7.2.1 Target position override 1 (RMV register)

Target position can be overridden by rewriting RMV register value during operation.

When performing acceleration/deceleration, set the slow-down point setting method to “RMD.MSDP = 0” (automatic setting).

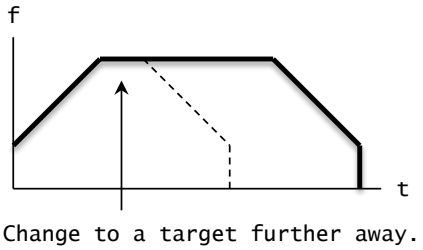
When the slow-down point setting method is “RMD.MSDP = 0” (automatic setting) and S-curve acceleration/ deceleration is set, there are the following restrictions. If you do not follow these restrictions, slow-down point automatic setting function cannot be performed.

If deceleration start is delayed, it stops before reaching FL speed. If deceleration starts earlier, movement at FL speed will be performed after deceleration is completed.

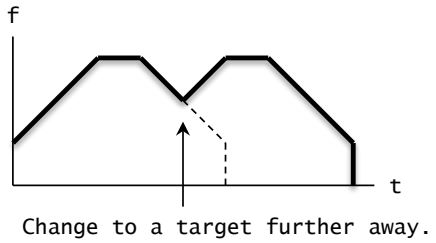
1. Do not override target positions during acceleration/deceleration.
2. Set to “RMD.MADJ = 1” (no triangle drive avoidance).

Target position override is performed based on the starting position.

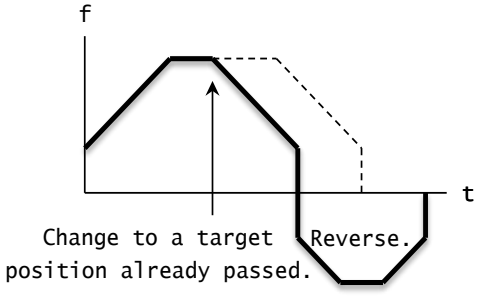
1) If the new target position is further away from the original target position during acceleration or constant speed operation, an operation with the same speed pattern will be performed and it will be completed at the new target position.



2) If the new target position is further away from the original target position during deceleration, re-acceleration is performed from the current position to FH speed and the positioning control is completed at the new target position.
If the current speed is Fu, the re-acceleration curve will be equal to a normal acceleration curve when RFL=Fu.



3) When passing through the new target position to the passed position or overriding the new target position closer than the initial target position while decelerating, operation reverses after deceleration stop and completes at the new target position.



Acceleration or deceleration operation can be performed only in high-speed start 1 and 2.

You can override the target position as often as possible, but please consider the restrictions carefully.

In the case of setting “RMD.MADJ = 0” (avoiding triangular drive), FH speed is corrected in relation to the initial target position. Even if you override the new target position further away from the initial target position, FH speed will not be corrected.

Note: Target position override can only be performed during operation.
If a target position override is performed just before stopping, the target position override may not be accepted.
Therefore, please confirm “MSTS.SEOR = 1” (stopped at other than the target position) after stopping.
See “4.2.1 Main-status (MSTS)” for details.

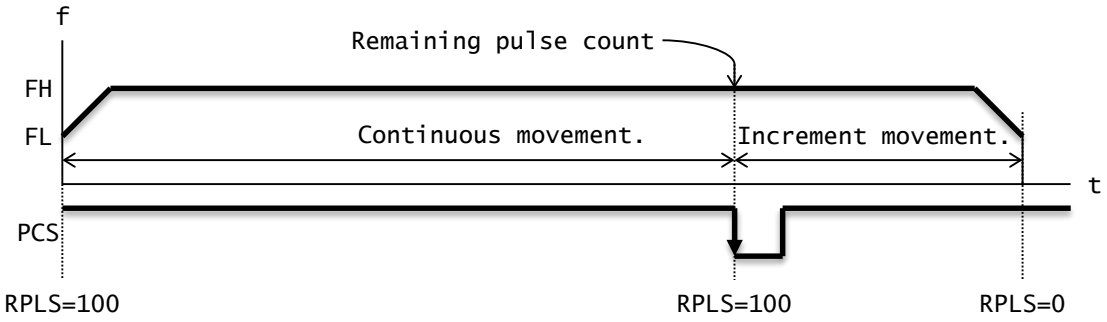
7.2.2 Target position override 2 (PCSn)

By setting “RENV1.PCSM = 1” and “RMD.MPCS = 1”, the operation will start like continuous movement operation mode.

If a pulse count start signal is input, a positioning control starts for the feeding amount set in RMV register.

Instead of inputting pulse count start signals, writing STAON command (28h) can start positioning control.

Input logic of PCSn terminal can be changed. PCSn terminal status can be read.



Target position override 2 <PRMD.MPCS(14)>

[PRMD] (R/W)

15 8
- n - - - - - -

Select the function of PCSn terminal
0: General-purpose input
1: Wait for input of pulse count start signal of target position override 2.
Performs like continuous movement operation mode until the pulse count start signal turns ON.
When “RENV1.PCSM = 1”, it becomes an input terminal of own-axis start signal.

RMD.MPCS	RENV1.PCSM	PCSn terminal
0	0	General-purpose input
0	1	Own-axis start
1	0	Pulse count start
1	1	Own-axis start

Input logic (PCSn) <RENV1.PCSL(24)>

[RENV1] (R/W)

31 24
- - - - - - - n

0: Negative logic
1: Positive logic

Input selection (PCSn) <RENV1.PCSM(30)>

[RENV1] (R/W)

31 24
- n - - - - - -

Select the function of PCSn and CSTA terminals.
0: Function selected by RMD.MPCS bit.
1: Own-axis start function.
It does not start even if simultaneous start signal is input to CSTA terminal.

RENV1.PCSM	RMD.MPCS	PCSn terminal	CSTA terminal
0	0	General-purpose input	Simultaneous start
0	1	Pulse count start	Simultaneous start
1	0	Own-axis start	Shared input
1	1	Own-axis start	Shared input

PCSn terminal status <RSTS.SPCS(8)>

[RSTS] (R)

15 8
- - - - - - - n

1: When “RMD.PCSL = 0”, “PCSn = L level”.
When “RMD.PCSL = 1”, “PCSn = H level”.

Pulse count start <STAON>

[Command]

28h

Starts positioning control of target position override 2.

7.3 Output pulse control

7.3.1 Output pulse mode (OUTn, DIRn)

For command pulse output modes, there are 4 types of common command pulse modes, 2 types of 2-pulse modes, and 2 types of 90-degree phase difference mode. Command pulse output modes are selected by RENV1.PMD bit.

Common pulse mode: Outputs the command pulses from OUTn terminal, and outputs the direction identification signal from DIRn terminal. (RENV.PMD = 000b to 011b)

2-pulse mode: Outputs the positive direction operation pulses from OUTn terminal, and outputs the negative direction operation pulses from DIRn terminal. (RENV.PMD = 100b, 111b)

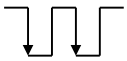
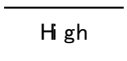
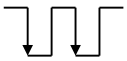
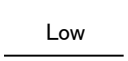
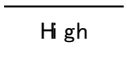
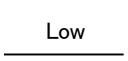
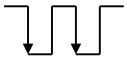
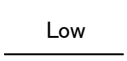
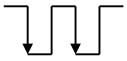
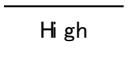
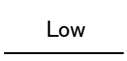
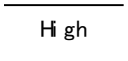
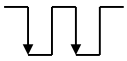
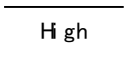
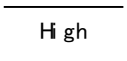
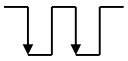
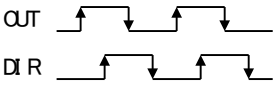
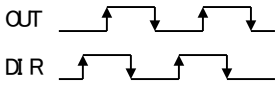
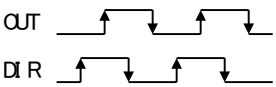
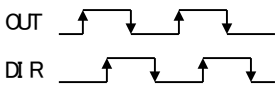
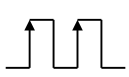
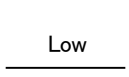
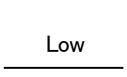
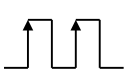
90-degree phase difference mode: Outputs A-phase pulse signal with 90-degree phase difference from OUTn terminal in 4 multiplication, and outputs the B-phase pulse signal of 90-degree phase difference from DIRn terminal in 4 multiplication. (RENV.PMD = 101b, 110b)

The direction change timer can be used when the motor driver that uses the common pulse mode needs time from the change of the direction signal until receiving the command pulse.

Output pulse mode <RENV1.PMD(2 to 0)>

[RENV1] (R/W)

7							0
-	-	-	-	-	n	n	n

PMD	Positive direction operation		Negative direction operation	
	OUT output	DIR output	OUT output	DIR output
000				
001				
10				
011				
100				
101				
110				
111				

Time of direction change timer <RENV1.DTMF(28)>

[RENV1] (R/W)

31							24
-	-	-	n	-	-	-	-

0: In common pulse mode, waits for 0.2 ms after the direction change.
1: In common pulse mode, waits for 0.5 µs after the direction change.

7.3.2 Output pulse width control and operation complete timing

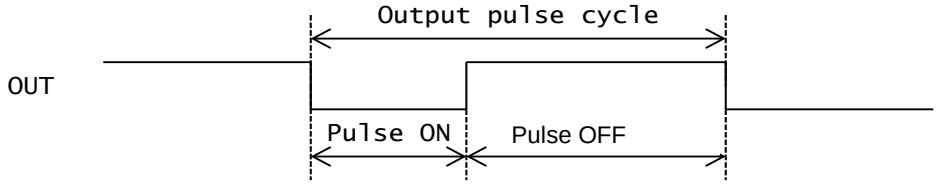
Change the output pulse width in accordance with the output pulse cycle of command pulses.

ON width of output pulse is 50% duty ratio.

When RMG register setting is an even number, an error occurs in the duty ratio, so that ON-time becomes shorter than OFF-time.

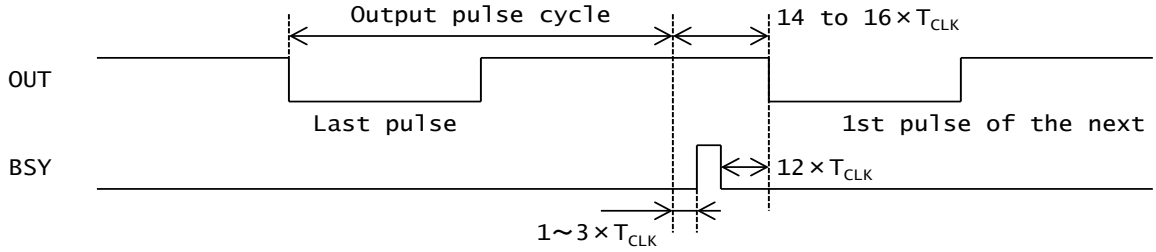
$$\frac{\text{Pulse ON time}}{\text{Output pulse cycle}} = \frac{\frac{\text{RMG}}{2}}{\text{RMG+1}}$$

For example, when RMG register is 2, the output pulse cycle is 3, and the pulse ON time becomes 1, so that the duty ratio becomes 1: 2.



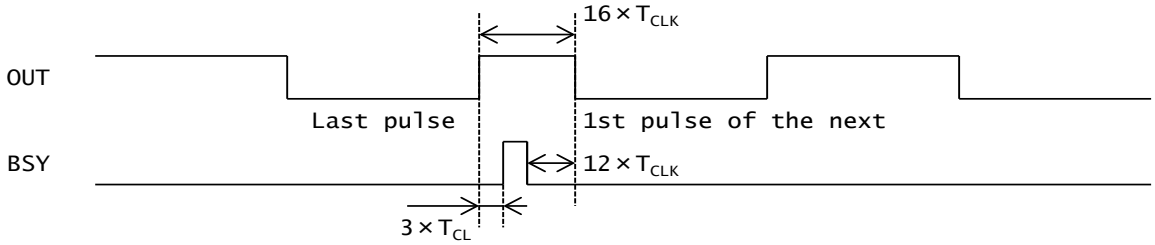
The operation complete timing can be changed by RMD.METM bit setting,

1) RMD.METM = 0 (When output pulse cycle is completed.)



(TCLK: Reference clock cycle)

2) RMD.METM = 1 (When output ON width is completed.)

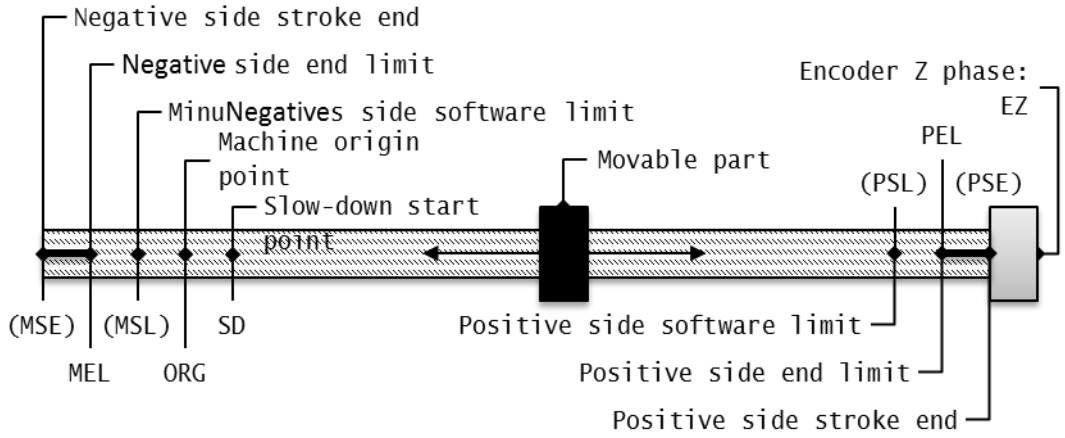


(T_{CLK}: Reference clock cycle)

Operation complete timing <PRMD.METM(12)>	[PRMD] (R/W)
0: Select “output pulse cycle is completed”. 1: Select “output ON width is completed”	15 … 8 - - - n - - - -

7.4 Mechanical input control

In addition to the end limit switches (PELn, MELn), the origin switch (ORGn), the slow-down switch (SDn), which are assembled in a machine like a slider in the figure below, Z-phase output (EZn) of the rotary encoder is used as an external input trigger in various operations.

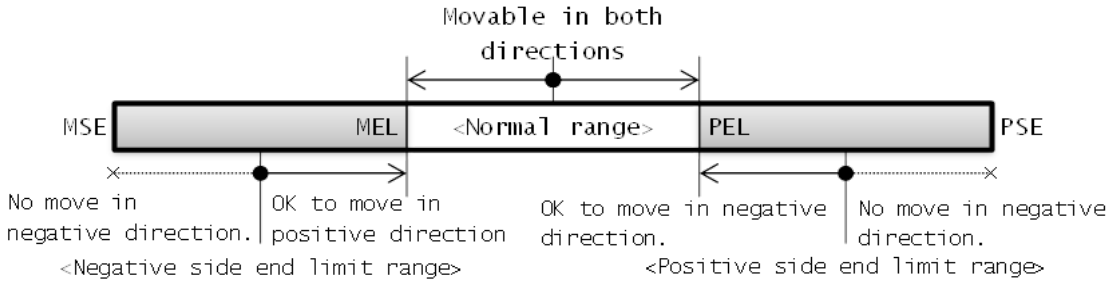


7.4.1 End limit signal (PELn, MELn)

Abnormal stops are performed when an end limit signal in positive direction turns ON during positive direction operations, or while the end limit in negative side turns ON during negative direction operations. You can select either immediate stops or deceleration stops.

If deceleration stop is selected, it stops after passing PEL position or MEL position.

It does not start in positive direction when end limit signal in positive direction is ON and does not start in negative direction when the negative direction is ON. For your safety, keep the end limit signal ON until the stroke end (PSE, MSE).



The input logic (ELLn terminal) and the input noise filter (RENV1.FLTR) can be selected for the positive side PELn terminal and the negative side MELn terminal that input the end limit signal.

The status of PELn and MELn terminals can be read by sub status (SSTS.SPEL, SSTS.SMEL).

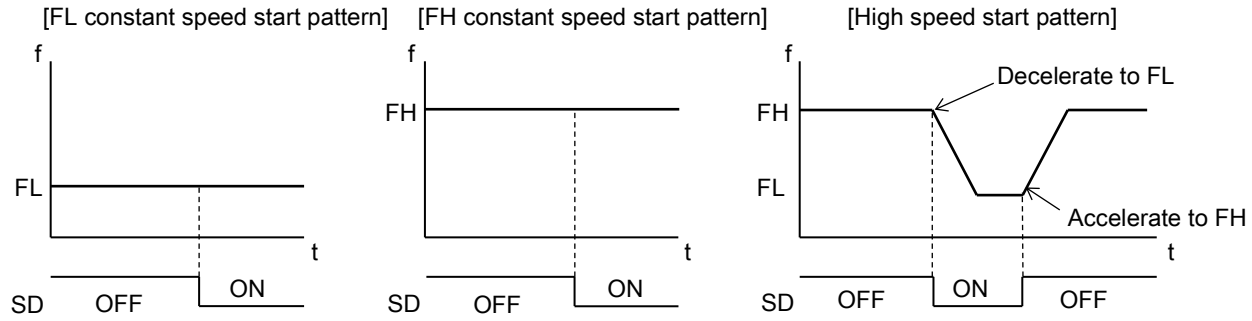
Input logic (PELn, MELn) <ELLn input terminal> L: Positive logic H: Negative logic	-
Stop method by input (PELn, MELn) <RENV1.ELM(3)> 0: Immediate stop 1: Decelerate and stop	[RENV1] (R/W) 7 0 - - - - n - - -
Input noise filter (PELn, MELn, SDn, ORGn, ALMn, INPn, CEMG) <RENV1.FLTR(26)> 0: Recognizes pulse width equals to 0.1 µs or wider. 1: Recognizes pulse width of the value set by RENV1.FTM bit or wider.	[RENV1] (R/W) 31 24 - - - - - n - -
Selects the input noise filter characteristics (PELn, MELn, SDn, ORGn, ALMn, INPn, CEMG) <RENV1.FTM(21, 20)> 00b: 3.2 µs 01b: 25 µs 10b: 200 µs 11b: 1.6 ms	[RENV1] (R/W) 23 16 - - n n - - - -
PELn terminal status <SSTS.SPEL(12)> 0: End limit signal in positive direction turns OFF. 1: End limit signal in positive direction turns ON.	[SSTS] (R) 15 8 - - - n - - - -
MELn terminal status <SSTS.SMEL(13)> 0: End limit signal in negative direction turns OFF. 1: End limit signal in negative direction turns ON.	[SSTS] (R) 15 8 - - n - - - - -
Obtains the error interrupt factor <REST.ESPL(0)> 1: Stopped by turning ON of the end limit signal in positive direction.	[REST] (R/W) 7 0 - - - - - - - n
Obtains the error interrupt factor <REST.ESML(1)> 1: Stopped by turning ON of the end limit signal in negative direction.	[REST] (R/W) 7 0 - - - - - - n -

7.4.2 Slow-down signal (SDn)

In case “PRMD.MSDE = 1” is set, operation will: 1) decelerate, 2) latch and decelerate, 3) decelerate and stop, or 4) latch and perform a deceleration stop when slow-down signal turns ON during an operation.

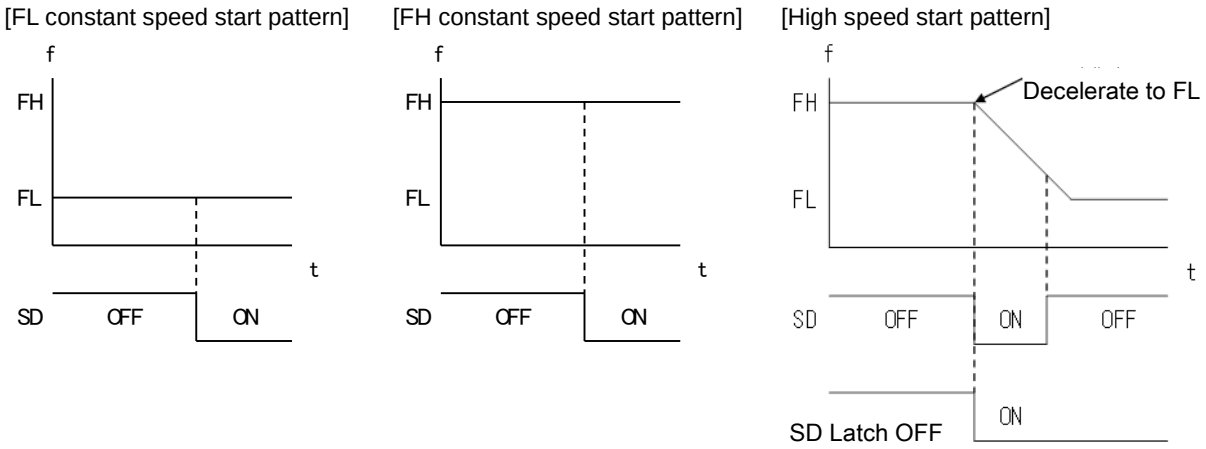
1) Deceleration <RENV1.SDM = 0, RENV1.SDLT = 0>

- While operating at constant speed pattern, slow-down signal is ignored.
- While in high speed start pattern, a motor decelerates to FL speed when slow-down signal turns ON.
  After decelerating, or while decelerating, the motor will accelerate to FH speed if slow-down signal turns OFF.
- If slow-down signal is being ON when STAD (52h) command or STAUD (53h) command is written, the motor will operate at FL speed. When slow-down signal turns OFF, the motor will accelerate to FH speed.



2) Latch and deceleration <RENV1.SDM = 0, RENV1.SDLT = 1>

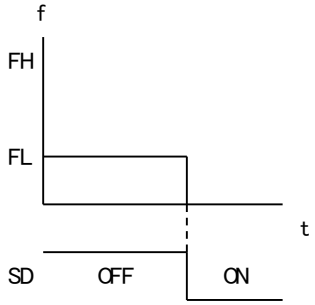
- While operating at constant speed pattern, slow-down signal is ignored.
- While in high speed start pattern, a motor decelerates to FL speed when slow-down signal turns ON.
  After decelerating, or while decelerating, the motor will not accelerate even if slow-down signal turns OFF.
- If slow-down signal is being ON when STAD (52h) command or STAUD (53h) command is written, the motor will operate at FL speed. Even if slow-down signal turns OFF, however, the motor will not accelerate to FH speed.



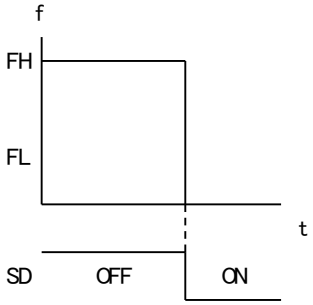
3) Deceleration stop <RENV1.SDM =1, RENV1.SDLT = 0>

- While operating at constant speed pattern, a motor will stop immediately if slow-down signal turns ON.
- While in high-speed start pattern, a motor will decelerate to FL speed and then stop when slow-down signal turns ON. If slow-down signal turns OFF during deceleration, it will accelerate to FH speed.
- If slow-down signal is being ON when writing a start command, an operation ends without starting.
- When stopped, an error interrupt (REST.ESSD) will occur.

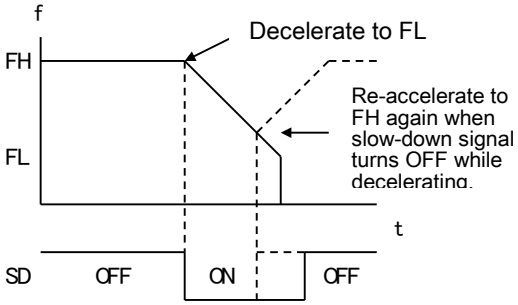
[FL constant speed start pattern]



[FH constant speed start pattern]



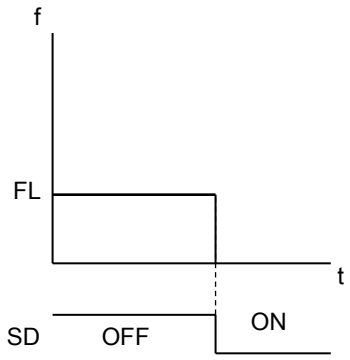
[High speed start pattern]



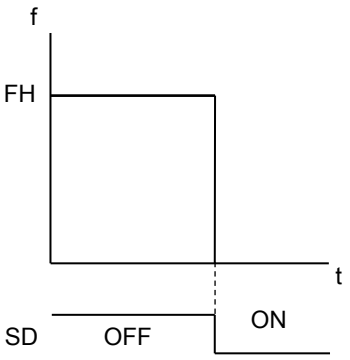
(4) Latch & deceleration stop <RENV1.SDM = 1, RENV1.SDLT = 1>

- While operating at FL constant speed start pattern, the motor will stop immediately when slow-down signal turns ON.
- While in high-speed start pattern, the motor will decelerate to FL speed and then stop when slow-down signal turns ON. Even if slow-down signal turns OFF during deceleration, the motor will not accelerate.
- If slow-down signal is being ON when writing a start command, the operation ends without starting.
- When stopped, an error interrupt (REST.ESSD) will occur.

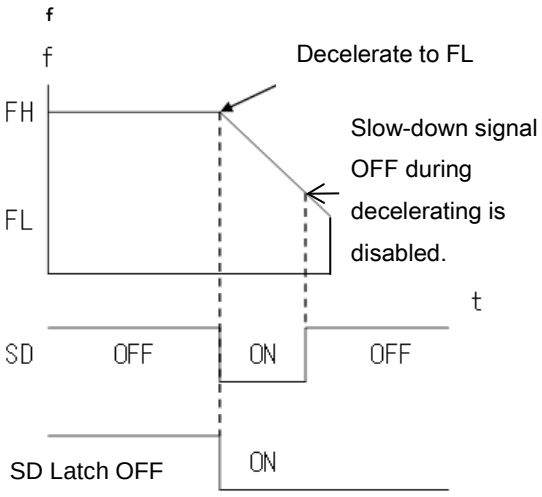
[FL constant speed star pattern]



[FH constant speed start pattern]



[High speed start pattern]



The input logic of SDn terminal can be changed.

If “RENV1.SDLT = 1” (latched input) is selected for slow-down signal input, the latch will be reset when SDn terminal is OFF at the following start.
The latch is also reset when “RENV1.SDLT = 0” (latch input release) is set again.

The minimum pulse width of slow-down signal is for 2 cycles of CLK signal (0.1 µs) when input noise filter of SDn terminal is OFF. When input noise filter of SDn terminal is ON, it recognizes a signal with a pulse width equal to or wider than the set time.

The slow-down latch signal can be read with sub status (SSTS.SSD), and the status of SDn terminal can be read with extension status (RSTS.SDIN). Also, it is possible to read the error interrupt factor caused by slow-down signal being turned ON with REST register.

Input function (SDn) <PRMD.MSDE(8)> Select the input function of slow-down signal. 0: General-purpose input. Status of SDn terminal can be obtained by RSTS.SDIN bit. 1: When SDn terminal turns ON, the motor decelerates or decelerates and stops.	[PRMD] (R/W) 15 8 - - - - - - - n
Input logic (SDn) <RENV1.SDL(6)> 0: Negative logic. 1: Positive logic.	[RENV1] (R/W) 7 0 - n - - - - - -
Input process (SDn) <RENV1.SDM(4)> 0: Decelerate. 1: Decelerate and stop.	[RENV1] (R/W) 7 0 - - - n - - - -
Input latch function (SDn) <RENV1.SDLT(5)> It can be used when the signal width with slow-down signal ON is short. 0: When slow-down signal is ON, slow-down latch signal is not turned ON. The status of SDn terminal can be obtained with RSTS.SDIN bit. 1: When slow-down signal is ON, slow-down latch signal turns ON. The slow-down latch signal status can be obtained by SSTS.SSD bit. When starting with slow-down signal OFF, slow-down latch signal turns OFF. Even when RENV1.SDLT = 0 is set, the slow-down latch signal turns OFF.	[RENV1] (R/W) 7 0 - - n - - - - -
Reads slow-down latch signal <SSTS.SSD(15)> 0: Slow-down latch signal is OFF. 1: Slow-down latch signal is ON.	[SSTS] (R) 15 8 n - - - - - - -
SDn terminal status <RSTS.SDIN(14)> 1: When “RMD.SDL = 0”, “SDn = L level”, When “RMD.SDL = 1”, “SDn = H level”.	[RSTS] (R) 15 8 - n - - - - - -

Obtain the error interrupt factor <REST.ESSD(5)> 1: Stopped by slow-down signal ON.	[REST] (R/W) 7 0 - - n - - - - -
Input noise filter (PELn, MELn, SDn, ORGn, ALMn, INPn, CEMG) <RENV1.FLTR(26)> 0: Recognizes pulse width of 0.1 µs or wider. 1: Recognizes pulse width equals to or wider than the value set by RENV1.FTM bit	[RENV1] (R/W) 31 24 - - - - - n - -
Input noise filter characteristics (PELn, MELn, SDn, ORGn, ALMn, INPn, CEMG) <RENV1.FTM(21, 20)> 00b: 3.2 µs 01b: 25 µs 10b: 200 µs 11b: 1.6 ms	[RENV1] (R/W) 23 16 - - n n - - - -

7.4.3 Origin position signal (ORGn), encoder Z-phase signal (EZn)

These signals are used in origin return control.

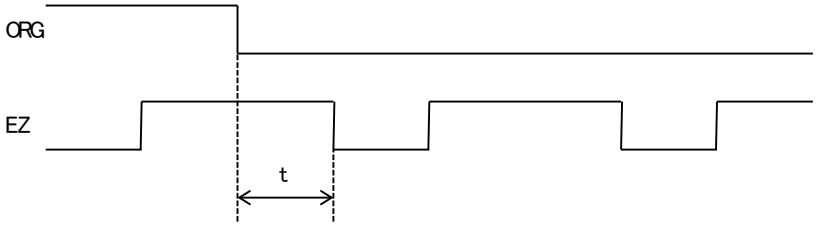
The minimum pulse width of origin signal requires two cycles (0.1 µs) of CLK signal when input noise filter of ORGn terminal is OFF. When input noise filter of ORGn terminal is ON, a signal with a pulse width equal to or wider than the set time is recognized.

The input logic of origin signal and encoder Z-phase signal is changed with RENV1 and RENV2 registers.

The status of ORGn terminal can be read with the sub status (SSTS.SORG).
The status of EZn terminal can be read with extension status (RSTS.SEZ).

For details on origin return control, see “5.5 Origin return control”.

<Timing when the origin signal is in negative logic, the encoder Z-phase signal is at falling edge, and the input noise filter is OFF>



1) When $t \geqq 2 \times T_{CLK}$ Counts
2) When $T_{CLK} < t < 2 \times T_{CLK}$ Not specified whether or not to count
3) When $t \leqq T_{CLK}$ Not count

T_{CLK}: Reference clock cycle

Operation mode <PRMD.MOD(6 to 0)> 0010000b (10h): Positive direction origin return control mode by origin return control 0011000b (18h): Negative direction origin return control mode by origin return control	[PRMD] (R/W) 7 0 0 n n n n n n n
Encoder Z-phase signal setting <RENV2.ORM(29)> 0: Selects origin return 0 operation mode that does not use encoder Z-phase signals. 1: Selects origin return 1 operation mode that uses encoder Z-phase signals.	[RENV2] (R/W) 3 2 1 4 - - n - - - - -
Input logic (ORGn) <RENV1.ORGL(7)> 0: Negative logic 1: Positive logic	[RENV1] (R/W) 7 0 n - - - - - - -
Input noise filter (PELn, MELn, SDn, ORGn, ALMn, INPn, CEMG) <RENV1.FLTR(26)> 0: Recognizes pulse width equals 0.1 µs or wider. 1: Recognizes pulse width of the value set by RENV1.FTM bit or wider.	[RENV1] (R/W) 31 24 - - - - - n - -
Input noise filter characteristics (PELn, MELn, SDn, ORGn, ALMn, INPn, CEMG) <RENV1.FTM(21, 20)> 00b: 3.2 µs 01b: 25 µs 10b: 200 µs 11b: 1.6 ms	[RENV1] (R/W) 23 16 - - n n - - - -
Reads an origin signal <SSTS.SORG(14)> 0: Origin signal is OFF. 1: Origin signal is ON.	[SSTS] (R) 15 8 - n - - - - - -
EZ count value used in origin return control <RENV2.EZD(27 to 24)> Setting range is 0000b (1st) to 1111b(16th)	[RENV2] (R/W) 31 24 - - - - n n n n
Encoder Z-phase signal input characteristic <RENV2.EZL(28)> 0: Falling edge. 1: Rising edge.	[RENV2] (R/W) 31 24 - - - n - - - -
EZn terminal status <RSTS.SEZ(10)> 1: “EZn = L level”	[RSTS] (R) 15 8 - - - - - n - -
Input noise filter (EZn, EBn, EZn) <RENV2.EINF(18)> 0: Recognizes pulse width equals to 0.1 µs or wider. 1: Recognizes pulse width of 0.15 µs or wider.	[RENV2] (R/W) 23 16 - - - - - n - -

7.5 Servo motor interface

Various controls can be performed by connecting with the in-position output (INP), deviation counter clear input (ERC) and alarm output (ALM) of servo motor drivers.

7.5.1 In-position signal (INPn)

The pulse-train input type servo drivers have deviation counters to count the difference between command pulse inputs and feedback pulse inputs. The drivers control servo motors so that the difference between command pulse inputs and feedback pulse inputs becomes zero. In other words, a servo motor operates later than the command pulses and, even after the command pulses stop, the servo motor systems keep operating until the count in the deviation counter reaches “0”.

Usually, an operation completes when the pulse output completes.
This can be delayed until the in-position signal from the servo motor driver is input to INPn terminal.
In this case, BSY signal, the main-status stop condition bits (MSTS.SSCM, MSTS.SRUN, MSTS.SENI, MSTS.SEND, MSTS.SERR, and MSTS.SINT) and extended status operation status (RSTS.CND) also changes when the in-position signal is input.

The minimum pulse width of the in-position signal requires two CLK signal cycles (0.1 µs) when the input noise filter of INPn terminal is OFF. When the input noise filter of INPn terminal is ON, a signal with a pulse width equal to or wider than the set time is recognized. Additionally, when the pulse output is completed, if in-position signal is already ON, the operation completes without delay.
The input logic of in-position signal can be changed.
The status of in-position signal can be read with the extended status (RSTS.SINP).

Input function(INPn) 0: General-purpose input INPn terminal status can be obtained by RSTS.SINP bit. 1: Operation completion is delayed until in-position signal turns ON.	<PRMD.MINP(9)>	[PRMD] (R/W) 15 … 8 - - - - - - n -
Input logic (INPn) 0: Negative logic 1: Positive logic	<RENV1.INPL(22)>	[RENV1] (R/W) 23 … 16 - n - - - - - -
INPn terminal status 1: When “RMD.INPL = 0”, “INPn = L level”, When “RMD.INPL = 1”, “INPn = H level”.	<RSTS.SINP(15)>	[RSTS] (R) 15 … 8 n - - - - - - -
Input noise filter (PELn, MELn, SDn, ORGn, ALMn, INPn, CEMG) 0: Recognizes pulse width equals to 0.1 µs or wider. 1: Recognizes pulse width of the value set by RENV1.FTM bit or wider.	<RENV1.FLTR(26)>	[RENV1] (R/W) 31 … 24 - - - - - n - -
Input noise filter characteristics (PELn, MELn, SDn, ORGn, ALMn, INPn, CEMG) 00b: 3.2 µs 01b: 25 µs 10b: 200 µs 11b: 1.6 ms	<RENV1.FTM(21, 20)>	[RENV1] (R/W) 23 … 16 - - n n - - - -

7.5.2 Deviation counter clear signal (ERCn)

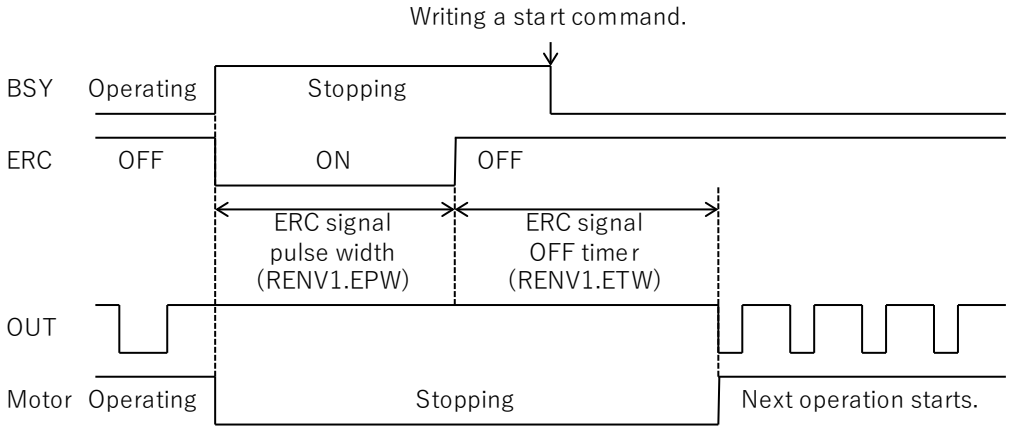
A servo motor does not stop until the deviation counter in a servo driver reaches “0”, even after command pulses have stopped being output. Therefore, even if the output of the command pulse is stopped, the immediate stop may not be performed in some cases.

In order to stop a servo motor immediately such as in an origin return control, the deviation counter needs to be cleared. Therefore, this LSI can output a signal from ERCn terminal to clear the deviation counter in a servo driver.

Even if a start command is written while stopping, command pulse output can wait from ON of a deviation counter clear signal until the deviation counter clear signal pulse width and the deviation counter clear signal OFF timer time. The pulse width (RENV1.EPW) of a deviation counter clear signal can be selected among the 5 types of one-shot pulse or level signal.

If a level signal is selected as the pulse width of a deviation counter clear signal (RENV1.EPW = 111b), turn it OFF with ERCRST (25h) command.

There is also a servo motor driver that requires a standby time (OFF timer) from turning off a deviation counter clear signal to accepting a command pulse. The deviation counter clear signal OFF timer (RENV1.ETW) can be selected from 4 different times.



In order to output a deviation counter clear signal at an abnormal stop, set RENV1.EROE = 1.

A deviation counter clear signal will not be output when the stop speed is at FL speed during FL constant speed drive or deceleration stop control. In the case of emergency stop, it outputs even when the stop speed is at FL speed.

Sets “RENV1.EROR = 1” in order to output a deviation counter clear signal at origin return.

Please refer to the waveforms of “5.5.1 Origin return 0 operation mode (RENV2.ORM = 0)” and “5.5.2 Origin return 1 operation mode (RENV2. ORM = 1)” for these timings.

ERC signal can be output by writing ERCOUT (24h) command. The output logic of deviation counter clear signal can be changed.

The status of ERCn terminal can be read with extension status (RSTS.SERC).

Output function at abnormal stop (ERCn) <RENV1.EROE(10)> [RENV1] (R/W)

The deviation counter clear signal can be output when stopped by turning ON PELn, MELn, ALMn, and CEMG terminals. Also, when stopped by writing CMEMG (05h) command.
0: Deviation counter clear signal ON is not output.
1: Deviation counter clear signal ON is output.

15							8
-	-	-	-	-	n	-	-

Output function at origin return (ERCn) <RENV1.EROR(11)> [RENV1] (R/W)

The deviation counter clear signal can be output when an origin return control completes.
0: Deviation counter clear signal ON is not output.
1: Deviation counter clear signal ON is output.

15							8
-	-	-	-	n	-	-	-

Pulse width (ERCn) <RENV1.EPW(14 to 12)> [RENV1] (R/W)

000b: 11 to 3 µs 001: 91 to 98 µs 010b: 360 to 390 µs 011b: 1.4 to 1.6 ms
100b: 11 to13 ms 101b: 46 to 50 ms 110b: 93 to 100 ms 111b: level output

15							8
-	n	n	n	-	-	-	-

Output logic (ERCn) <RENV1.ERCL(15)> [RENV1] (R/W)

0: Negative logic
1: Positive logic

15							8
n	-	-	-	-	-	-	-

OFF timer time (ERCn) <RENV1.ETW(17, 16)> [RENV1] (R/W)

00b: 0 µs 01b: 11 to 13 µs 10b: 1.4 to 1.6 ms 11b: 93 to 100 ms

23						16	
-	-	-	-	-	-	n	n

ERCn terminal status <RSTS.SERC(9)> [RSTS] (R)

1: When “RMD.ERCL = 0”, “ERCn = L level”.
When “RMD.ERCL = 1”, “ERCn = H level”.

15							8
-	-	-	-	-	-	n	-

Output command of deviation counter clear signal <ERCOUT> [Command]

A deviation counter clear signal is output from ERCn terminal. 24h

Reset command for output of deviation counter clear signal <ERCRST> [Command]

Reset outputs from ERCn terminal. 25h

7.5.3 Alarm signals (ALMn)

Inputs alarm signal to ALMn terminal.

When alarm signal turns ON while in operation, the motor will stop immediately or decelerate and stop.

For constant speed pattern, only “stop immediately” is available.

In high speed patter, the choice can be made to stop immediately or to decelerate and stop.

If an alarm signal is ON, THE LSIA will not output any pulses even when a start command is written.

The minimum pulse width of the alarm signal requires 2 cycles of the reference clock (0.1 us) when the input noise filter of ALMn terminal is OFF.

The input logic of alarm signal can be changed.

The status of alarm signal can be monitored by reading sub status.

Input process (ALMn) <RENV1.ALMM(8)> 0: Immediate stop 1: Decelerate and stop	[RENV1] (R/W) 15 8 - - - - - - - n
Input logic (ALMn) <RENV1.ALML(9)> 0: Negative logic 1: Positive logic	[RENV1] (R/W) 15 8 - - - - - - n -
ALMn terminal status <SSTS.SALM(11)> 0: ALMn terminal is OFF. 1: ALMn terminal is ON.	[SSTS] (R) 15 8 - - - - n - - -
Obtains the error interrupt factor <REST.ESAL(2)> 1: Stopped by alarm signal ON, or alarm signal ON while stopping.	[REST] (R/W) 7 0 - - - - - n - -
Input noise filter (PELn, MELn, SDn, ORGn, ALMn, INPn, CEMG) <RENV1.FLTR(26)> 0: Recognizes pulse width equals 0.1 µs or wider. 1: Recognizes pulse width of the value set by RENV1.FTM bit or wider.	[RENV1] (R/W) 31 24 - - - - - n - -
Input noise filter characteristics (PELn, MELn, SDn, ORGn, ALMn, INPn, CEMG) <RENV1.FTM(21, 20)> 00b: 3.2 µs 01b: 25 µs 10b: 200 µs 11b: 1.6 ms	[RENV1] (R/W) 23 16 - - n n - - - -

7.6 Simultaneous start

7.6.1 Simultaneous start signal (CSTA)

When connecting CSTA terminal, multi axes can be started simultaneously.

Writing CMSTA (06h) command enables to output a negative logic one-shot pulse from CSTA terminal.

When “CSTA = L level”, multi axes that have waited for a simultaneous start input, can be started simultaneously.

When “CSTA = L level”, an event interrupt can be generated.

You can select either “RENV1.STAM = 0” (level trigger) or “RENV1.STAM = 1” (edge trigger) for simultaneous start signal input specifications,

If “CSTA = L level” with “RENV1.STAM = 0” (level trigger), writing a start command will start an operation immediately. The status of CSTA terminal can be checked with extension status (RSTS.SSTA).

<How to perform simultaneous starts>

Sets “PRMD.MSY = 01b” for the axes to start simultaneously.

Then, when a start command is written, it becomes the input wait state (RSTS.CND = 0010b) of simultaneous start signals. Then, you can simultaneously start by the following two methods:

1) Writes a simultaneous start command.

The LSI will output one shot signal of 8 CLK (reference clock) cycles (0.4 µs) from CSTA terminal.

Other axes start by inputting one-shot pulse. Own-axis starts by re-inputting the output one-shot pulse.

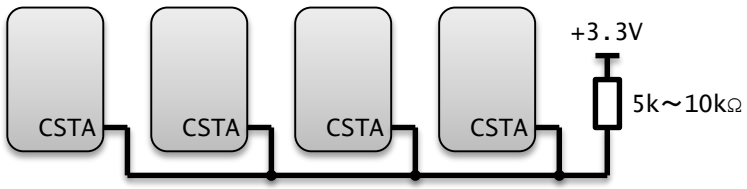
2) Inputs a hardware signal from outside.

Supplies a hardware signal after driving the terminal with open drain output (SN74LVC2G06 or equivalent).

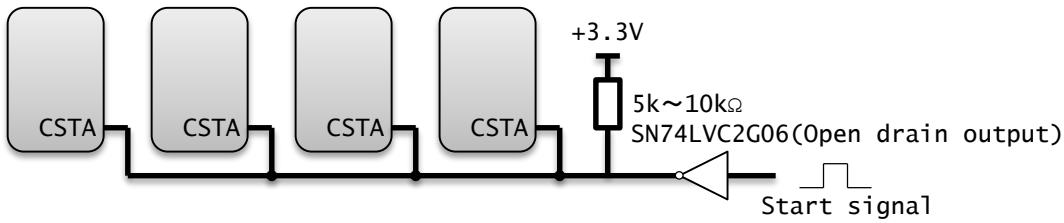
When waiting for simultaneous start signal input (RSTS.CND = 0010b), each axis can be started individually with SPSTA (2Ah) command.

Even when CSTA terminal is connected, if “PRMD.MSY = 00b” is set, each axis can be started individually

1. To perform a simultaneous start, connect the LSIs as follows.



2. To start simultaneously from an external circuit as an external start, connect the LSIs as follows.



For simultaneous start signal, input one-shot pulse whose pulse width is equal to or wider than 4 CLK signals (0.2 µs).

Waiting for input <PRMD.MSY(19, 18)> 01b: If “RENV1.PCSM = 0”, it starts with “CSTA = L level” or with SPSTA (2Ah) command. If “RENV1.PCSM = 1”, it starts with PCSn terminal ON or with SPSTA (2Ah) command.	[PRMD] (R/W) 23 16 - - - - n n - -
Specifies Input specification (CSTA) <RENV1.STAM(18)> 0: Level trigger 1: Edge trigger	[RENV1] (R/W) 23 16 - - - - - n - -
CSTA terminal status <RSTS.SSTA(5)> 1: “CSTA = L level”	[RSTS] (R) 7 0 - - n - - - - -
Obtains the operation status. <RSTS.CND(3 to 0)> 0010b: Waiting for simultaneous start signal input.	[RSTS] (R) 7 0 - - - - n n n n
Sets the event interrupt factor. <RIRQ.IRSA(12)> 1: When it changes to “CSTA = L level”, an interrupt occurs.	[RIRQ] (R/W) 15 8 - - - n - - - -
Obtains the event interrupt factor <RIST.ISSA(13)> 1: It changed to “CSTA = L level”.	[RIST] (R/W) 15 8 - - n - - - - -
Simultaneous start command <CMSTA> A one-shot pulse of negative logic is output from CSTA terminal. This signal also serves as the input to CSTA terminal. If simultaneous start signal is waiting to be input, the own-axis will also start.	[Command] 06h
Own-axis start command <SPSTA> Simultaneous start signal is not output from CSTA terminal; only own-axis starts.	[Command] 2Ah

7.6.2 Own-axis start signal (PCSn)

When “PRMD.MSY = 01b” and “RENV1.PCSM = 1” are selected, only the own-axis can be started by inputting the own-axis start signal to PCSn terminal.

If “RENV1.PCSM = 1” is selected, it will not start with simultaneous start signal input to CSTA terminal.

You can start by writing SPSTA (2Ah) command.

The input logic of PCSn terminal can be changed.

The status of PCSn terminal can be confirmed with extension status (RSTS.SPCS).

Waiting for input <PRMD.MSY(19, 18)>

01b: If “RENV1.PCSM = 0”, it starts with “CSTA = L level" or with SPSTA (2Ah) command.
If “RENV.PCSM = 1”, it starts with PCSn terminal ON or with SPSTA (2Ah) command.

[PRMD] (R/W)

23							16
-	-	-	-	n	n	-	-

Input logic (PCSn) <RENV1.PCSL(24)>

0: Negative logic
1: Positive logic

[RENV1] (R/W)

31							24
-	-	-	-	-	-	-	n

Input selection (PCSn) <RENV1.PCSM(30)>

Select the functions of PCSn terminals and CSTA terminals.
0: Select the function by RMD.MPCS bit.
1: Own-axis start function.
It will not start even if simultaneous start signal is input to CSTA terminal.

[RENV1] (R/W)

31							24
-	n	-	-	-	-	-	-

RENV1.PCSM	RMD.MPCS	PCSn terminal	CSTA terminal
0	0	General-purpose input	Simultaneous start
0	1	Starts pulse count	Simultaneous start
1	0	Starts own-axis	Shared input
1	1	Starts own-axis	Shared input

PCSn terminal status <RSTS.SPCS(8)>

1: When “RMD.PCSL = 0”, “PCSn = L level”,
When “RMD.PCSL = 1”, “PCSn = H level”.

[RSTS] (R)

15							8
-	-	-	-	-	-	-	n

Own-axis start command <SPSTA>

Simultaneous start signal is not output from CSTA terminal; only own-axis starts.

[Command]

2Ah

7.7 Simultaneous deceleration

7.7.1 Simultaneous slow-down signal (CSD)

When CSD terminal is connected, multiple axes can be simultaneously decelerated by linear interpolation operation.

“CSD = L level” can be output during FL constant speed or deceleration. (PRMD.MCDO = 1)

When “CSD = L level” is input, the target speed can be changed to FL speed. (PRMD.MCDE = 1)

The input logic of CSD terminal cannot be changed.

The status of CSD terminal can be confirmed by extension status (RSTS.SCSD).

<How to perform simultaneous decelerations>

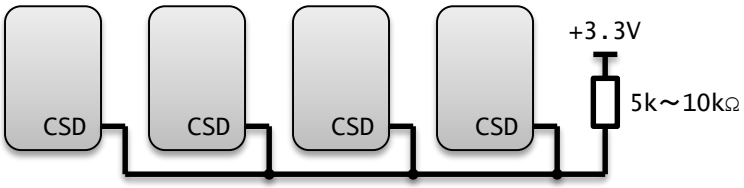
Sets “PRMD.MCDE = 1” for each of the axes that decelerates simultaneously and start.

Then, decelerate either interpolation axis by inputting a slow-down signal or others.

The interpolation axis during FL constant speed operation or during deceleration will output “CSD = L level”. (RMD.MCDO = 1)

For other interpolation axes, turn ON simultaneous slow-down signal input and change the target speed to FL speed in order to decelerate. (RMD.MCDE = 1)

To perform simultaneous decelerations, connect the LSIs as follows:



Input function (CSD) <PRMD.MCDE(28)> You can decelerate own-axis by a deceleration start of the other axis. 0: General-purpose input. The status of CSD terminal can be acquired with RSTS.SCSD bit. 1: The target speed is changed to FL speed when “QCSD = L level”.	[PRMD] (R/W) 31 24 0 0 - n 0 - - -
Output process (CSD) <PRMD.MCDO(29)> Deceleration of the other axis can start when the own-axis starts to decelerate. 0: Simultaneous slow-down signal is not output from CSD terminal during deceleration of own-axis or during FL constant speed operation. 1: Simultaneous slow-down signal is output from CSD terminal during deceleration of own-axis or during FL constant speed operation.	[PRMD] (R/W) 31 24 0 0 n - 0 - - -
CSD terminal status <RSTS.SCSD(4)> 1: “CSD = L level”.	[RSTS] (R) 7 0 - - - n - - - -

7.8 Simultaneous stop

7.8.1 Simultaneous stop signal (CSTP)

Multiple axes can be stopped at the same time if the CSTP terminals are connected.

“CSTP = L level” can be output when writing CMSTP (07h) command or occurring abnormal stops. (PRMD.MSPO = 1)

When “CSTP = L level”, stop immediately if “RENV1.STPM = 0” or decelerate and stop if “RENV1.STPM = 1”. (PRMD.MSPE=1)

An error interrupt (REST.ESSP) will occur when stopped at “CSTP = L level”.

The input logic of CSTP terminal cannot be changed.

The status of CSTP terminal can be confirmed with extension status (RSTS.SSTP).

<How to perform simultaneous stops>

Set PRMD.MSPE = “1” for each of the axes to stop simultaneously and start.

It stops simultaneously in any of the following three cases:

1) Writing CMSTP (07h) command

One-shot pulse with a pulse width of 8 cycles (0.4 µs) of the CLK signal is output from CSTP terminal. (RMD.MSPO = 1)

Own-axis is stopped by re-entering the output “CSTP = L level”. For other axes, “CSTP = L level” is input to stop.

2) Supply an external hardware signal

Input a hardware signal after driving the terminal with an open drain output (SN74LVC2G06 or equivalent).

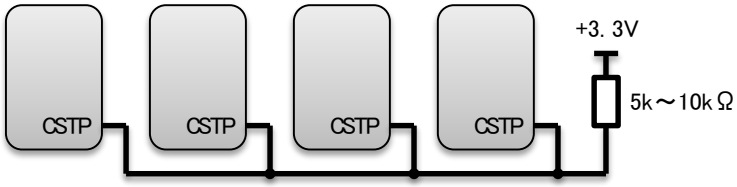
3) Abnormal stop of axis that is set to output “CSTP = L level”

One-shot pulse with a pulse width of 8 cycles (0.4 µs) of CLK signal is output from CSTP terminal. (RMD.MSPO = 1)

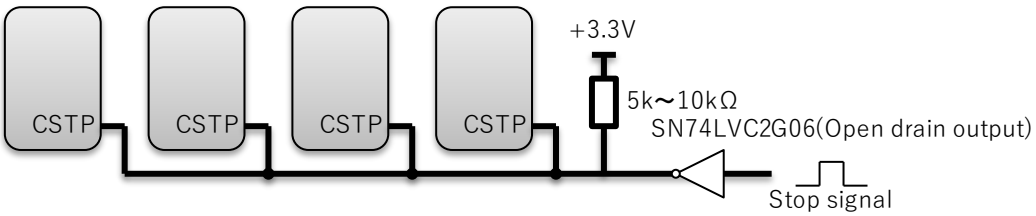
For other axes, “CSTP = L level” is input to stop.

Even when CSTP terminal are connected, each axis can be stopped individually by stop command.

1. To perform simultaneous stop, connect the LSIs as follows.



2. To stop simultaneously from an external circuit, connect the LSIs as follows.



For simultaneous stop signal, input one shot pulse whose pulse width is equal to or wider than 4 CLK signal (0.2 µs).

Input function (CSTP) <PRMD.MSPE(24)>

Stops own-axis with abnormal stop of other axes.
0: General-purpose input.
CSTP terminal status can be obtained by RSTS.SSTP bit.
1: Input simultaneous stop signal to CSTP terminal to decelerate & stop or stop immediately.

[PRMD] (R/W)

31							24
0	0	-	-	-	-	-	n

Input process (CSTP) <RENV1.STPM(19)>

0: Immediately stop
1: Decelerate and stop.

[RENV1] (R/W)

23							16
-	-	-	-	n	-	-	-

Outputs at abnormal stop function (CSTP) <PRMD.MSPO(25)>

Stops other-axis with abnormal stop of own-axis.
0: A one-shot pulse of negative logic is not output from CSTP terminal at abnormal stop of own-axis. Even in this case, it is possible to output a negative logic one shot pulse with CMSTP (07h) command.
1: A one-shot pulse of negative logic is output from CSTP terminal at abnormal stop of the own-axis.

[PRMD] (R/W)

31							24
0	0	-	-	-	-	n	-

Output by stop command function <RENV2.CSPO(13)>

The other axis can be stopped by stopping the own-axis by a stop command.
0: Negative logic one-shot pulse is not output from CSTP terminal by stopping the own-axis with stop command.
1: Negative logic one-shot pulse is output from CSTP terminal by stopping the own-axis with stop command. The condition is “RMD.MSPO = 1”.

[RENV2] (R/W)

15							8
-	-	n	-	-	-	-	-

CSTP terminal status <RSTS.SSTP(6)>

1: “CSTP = L level”

[RSTS] (R)

7							0
-	n	-	-	-	-	-	-

Obtains the error interrupt factor <REST.ESSP(3)>

1: Stopped at input of simultaneous stop signal.

[REST] (R/W)

7							0
-	-	-	-	n	-	-	-

Simultaneous stop command <CMSTP>

A negative logic one-shot pulse is output from CSTP terminal.
This signal also serves as the input to CSTP terminal.
If the simultaneous stop signal is set, own-axis is also stopped.

[Command]

07h

7.9 Emergency stop

7.9.1 Emergency stop signal (CEMG)

When CMEMG (05h) command is written or CEMG = L level, all the axes will stop emergently.

At an abnormal stop, error interrupt (REST.ESEM) will occur.

When error interrupt (REST.ESEM) on all axes, including stopped or unused, are cleared, it becomes “INT = H level”.

While CEMG = L level, no axis will operate.

The logic of CEMG signal input terminal cannot be changed.

The status of CEMG signal input terminal can be confirmed by extension status (RSTS.SEMG).

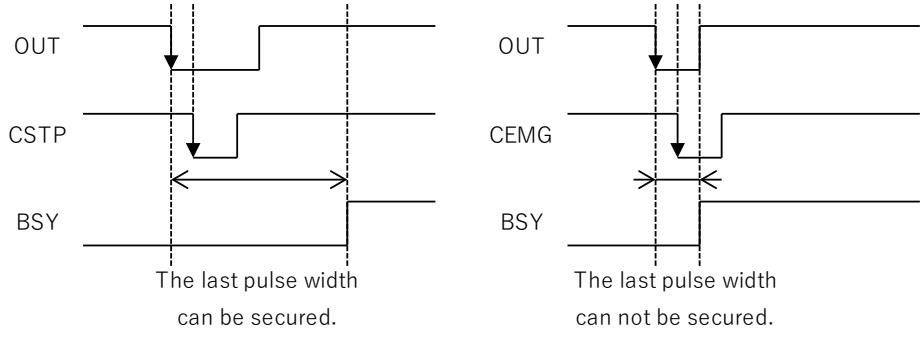
CEMG terminal status <RSTS.SEMG(7)> 1: “CEMG = L level	[RSTS] (R) 7 0 n - - - - - - -
Obtains an error interrupt factor <REST.ESEM(4)> 1: “CEMG = L level”, or CMEMG (05h) command is written.	[REST] (R/W) 7 0 - - - n - - - -
Emergency stop command <CMEMG> Emergency stop of the all axes and exits the operations mode.	[Command] 05h
Input noise filter (PELn, MELn, SDn, ORGn, ALMn, INPn, CEMG) <RENV1.FLTR(26)> 0: Recognizes pulse width equal to 0.1 µs or wider. 1: Recognizes pulse width of the value set by RENV1.FTM bit or wider.	[RENV1] (R/W) 31 24 - - - - - n - -
Input noise filter characteristics (PELn, MELn, SDn, ORGn, ALMn, INPn, CEMG) <RENV1.FTM(21, 20)> 00b: 3.2 µs 01b: 25 µs 10b: 200 µs 11b: 1.6 ms	[RENV1] (R/W) 23 16 - - n n - - - -

Note: In emergency stop operations, the final pulse width cannot be secured, and it may become spike-shaped.

When it becomes spike-shaped, the command position and machine position may not match.

(The motor driver does not accept, only the command position counter counts.)

Therefore, after emergency stop, return to origin position and match the command position with the machine position.



7.10 Counters

7.10.1 Counter type and input specification

The LSI has three built-in counters; one in-position counter (RPLS) and two counters (RCUN 1, RCUN 2) per axis. The positioning counter copies the absolute value of RMV register at start and counts down at every command pulse output. While "RMD.MPCS = 1" (target position override 2) is being executed, it does not count down until pulse count start signal is input.

	COUNTER 1 (RCUN1)	COUNTER 2 (RCUN2)	In-position Counter (RPLS)
Counter type	Up/down counter		Down counter
Bit length	32		32
Command pulse	Enabled to input		(For remaining pulse only)
Encoder signal (EAn, EBn)	Enabled to input		-

Inputs for counter 1 (RCUN 1) and counter 2 (RCUN 2) can be selected as in the table below.

Target of COUNTER 1(RCUN1) <RENV3.CIS1(0)> 0: Command position (Command pulse) 1: Mechanical position (Encoder signal)	[RENV3] (R/W) 7 0 - - - - - - - n
Target of COUNTER 2(RCUN2) <RENV3.CIS2(1)> 0: Mechanical position (Encoder signal) 1: Command position (Command pulse)	[RENV3] (R/W) 7 0 - - - - - - n -

The input specification of the encoder signal is selected from the two ways as follows:

Input specification	Counting direction
90-degree phase difference mode; 1, 2 and 4 multiplication.	Count when the phase of EA input is advanced. Count down when the phase of EB input is advanced.
2-pulse mode	Count at the rising edge of EA input. Count down at the rising edge of EB input

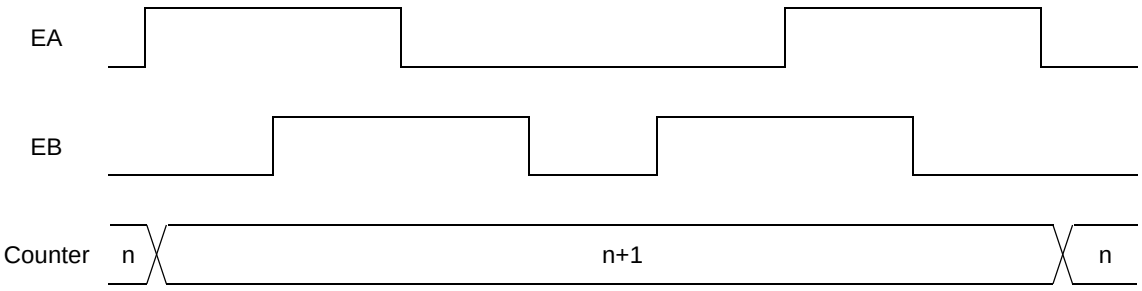
The counting direction of encoder signals can be reversed to the above.

In 90-degree phase difference mode, an error interrupt (REST.ESEE) occurs when EA terminal and EB terminal change at the same time. In 2-pulse mode, an error interrupt (REST.ESEE) occurs when EA signal and EB signal rise at the same time.

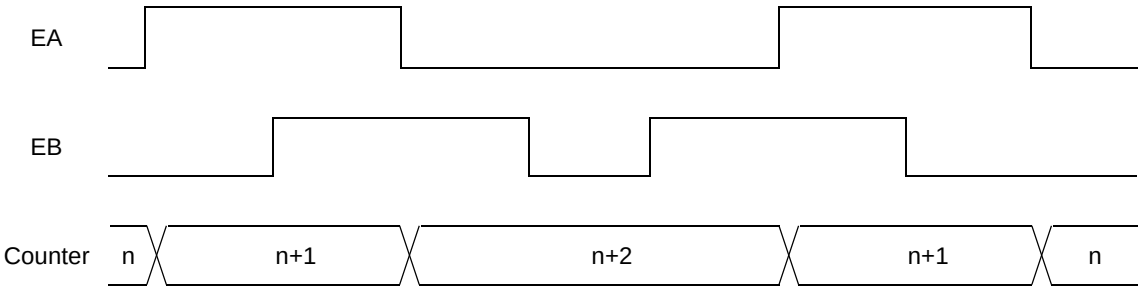
Input noise filter(EAn, EBn, EZn) <RENV2.EINF(18)> Selects the noise filter of EAn, EBn, EZn terminals. 0: Recognizes signals with a pulse width of 0.1 µs or wider. 1: Recognizes signals with a pulse width of 0.15µs or wider.	[RENV2] (R/W) 23 16 - - - - - n - -
Input specification (EAn, EBn) <RENV2.EIM(17, 16)> 00b: 90-degree phase difference mode of 1 multiplication is selected. 01b: 90-degree phase difference mode of 2 multiplication is selected. 10b: 90-degree phase difference mode of 4 multiplication is selected. 11b: 2-pulse mode is selected.	[RENV2] (R/W) 23 16 - - - - - - n n
Reverse counting direction (EAn, EBn) <RENV2.EDIR(19)> 0: Becomes forward direction 1: Becomes reverse direction	[RENV2] (R/W) 23 16 - - - - n - - -
Input stop (EAn, EBn) <RENV2.EOFF(14)> Set input function of EAn and EBn terminals 0: Input of encoder signal is enabled 1: Input of encoder signal is disabled It does not detect input errors.	[RENV2] (R/W) 15 8 - n - - - - - -
Obtains the error interrupt factor <REST.ESEE(7)> 1: Encoder signal input error occurred	[REST] (R/W) 7 0 n - - - - - - -

When RENV2.EDIR = 0, encoder signal (EA/EB) input and count timing will be as follows.

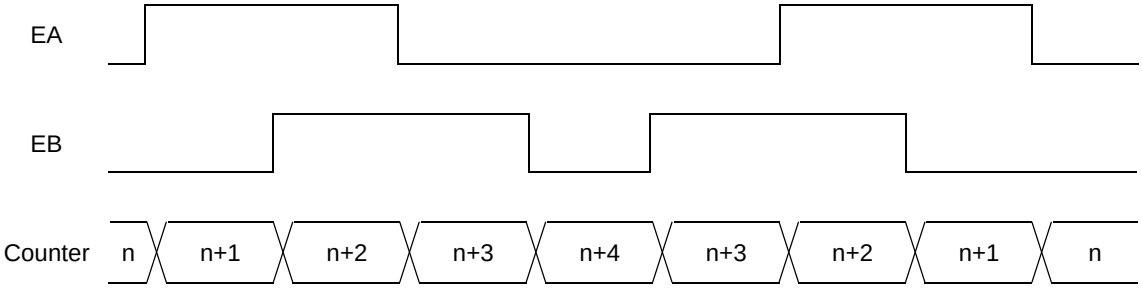
1) When using input of 90-degree phase difference mode of 1 multiplication.



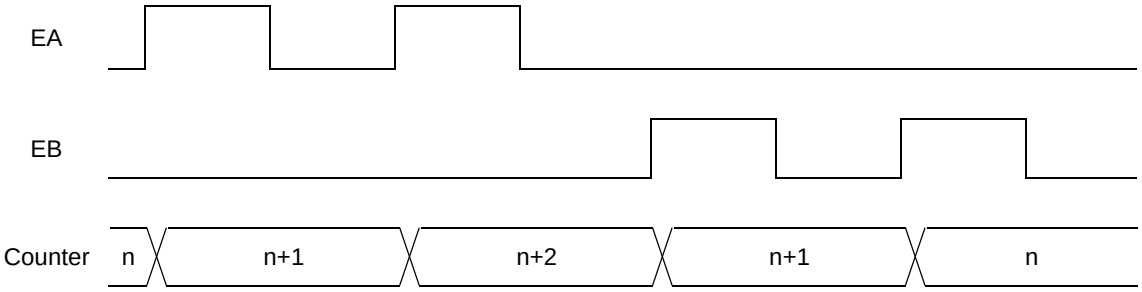
2) When using input of 90-degree phase difference mode of 2 multiplication.



3) When using input of 90-degree phase difference mode of 4 multiplication.



4) When using 2-pulse input (counted on the rising edge from L to H).



7.10.2 Latch and clear (LTCn)

7.10.2.1 Latch 1 and 2

RLTC1 register can latch, or latch & clear the Counter 1 in three ways. RLTC2 register can latch, or latch & clear the Counter 2 in three ways.

1. When the counter latch signal to LTCn terminal is ON
2. When ORGn terminal is ON, or when EZn terminal is ON with origin return control.
3. Write LTCH (29h) command

Input latch signal input specification can be selected with RENV1 register.

The latch timing can be selected with RENV3 register.

An event interrupt (RIST.ISLT) can be generated when counter latch signal is ON and RCUN 1 register value is latched into RLTC 1 register.

An event interrupt (RIST.ISLT) can also be generated when RCUN 2 register value is latched into RLTC2 register.

An event interrupt (RIST.ISOL) can be generated when origin signal is ON and RCUN 1 register value is latched into RLTC1 register.

An event interrupt (RIST.ISOL) can also be generated when RCUN 2 register value is latched into RLTC2 register.

Counters 1 and 2 can be latched and cleared by writing CUN1R (20h) command or CUN2R (21h) command.

It can also be latched and cleared even when the counter latch signal is ON.

If it is necessary to clear counters 1 and 2 by an external signal, use the input of counter latch signal.

Input specification (LTCn) <RENV1.LTCL(23)> 0: Falling edge. 1: Rising edge.	[RENV1] (R/W) 23 16 n - - - - - - -
LTCn terminal status <RSTS.SLTC(13)> 1: When “RENV1.LTCL = 0”, “LTCn = L level” When “RENV1.LTCL = 1”, “LTCn = H level”	[RSTS] (R) 15 8 - - n - - - - -
RLTC1 register counter latch by latch signal <RENV3.LOF1(5)> 0: Latched by input of counter latch signal. 1: Not latched by input of counter latch signal.	[RENV3] (R/W) 7 0 - - n - - - - -
Latch RLTC1 register by origin return control. <RENV3.CU1R(6)> 0: Not latched by origin return control. 1: Latched by origin return control.	[RENV3] (R/W) 7 0 - n - - - - - -
Counter 1 (RCUN1) clear when latching to RLTC1 register. <RENV3.CU1L(4)> 0: Counter 1 (RCUN1) is not cleared simultaneously when latching to RLTC1 register. 1: Counter 1 (RCUN1) is cleared simultaneously when latching to RLTC1 register.	[RENV3] (R/W) 7 0 - - - n - - - -
RLTC2 register counter latch by latch signal <RENV3.LOF2(9)> 0: Latched by input of counter latch signal. 1: Not latched by input of counter latch signal.	[RENV3] (R/W) 15 8 - - - - - - n -
Latch RLTC2 register by origin return control. <RENV3.CU2R(10)> 0: Not latched by origin return control. 1: Latched by origin return control.	[RENV3] (R/W) 15 8 - - - - - n - -
Counter 2 (RCUN2) clear when latching to RLTC2 register. <RENV3.CU2L(8)> 0: Counter 2 (RCUN2) is not cleared simultaneously when latching to RLTC2 register. 1: Counter 2 (RCUN2) is cleared simultaneously when latching to RLTC2 register.	[RENV3] (R/W) 15 8 - - - - - - - n
Sets the event interrupt factor. <RIRQ.IRLT(8)> 1: An interrupt is generated by latching the count value by inputting counter latch signal. The target is RLTC1 register or RLTC2 register. If “RENV3.LOF1 = 1” and “RENV3.LOF2 = 1”, no interrupt is generated.	[RIRQ] (R/W) 15 8 - - - - - - - n
Obtains the event interrupt factor <RIST.ISLT(8)> Count value is latched by counter latch signal input.	[RIST] (R/W) 15 8 - - - - - - - n
Sets the event interrupt factor <RIRQ.IROL(9)> 1: When origin position signal turns ON, interrupt is generated. When “RENV3.CU1R = 0” and “RENV3.CU2R = 0”, no interrupt is generated. This interrupt also occurs in operation modes other than origin return control.	[RIRQ] (R/W) 15 8 - - - - - - n -

Obtains the event interrupt factor <RIST.ISOL(9)> 1: Origin position signal turns ON.	[RIST] (R/W) 15 8 - - - - - - n -
Counter 1 clear command <CUN1R> Clear counter 1 (RCUN1).	[Command] 20h
Counter 2 clear command <CUN2R> Clear counter 2 (RCUN2).	[Command] 21h
Counter 1 & 2 latch command <LTCH> RCUN1 register value is latched in RLTC1 register and RCUN2 register value is latched in RLTC2 register.	[Command] 29h

Note: When “RENV3.CU1L = 1” is set, RCUN1 register value after resetting may become “+1” or “-1”.
When “RENV3.CU2L = 1” is set, RCUN2 register value after resetting may become “+1” or “-1”.
Be careful when detecting “0” by a comparator function.

7.10.2.2 Latches 3 and 4

RLTC3 register can latch counter 1 or counter 2 in seven different ways.

RLTC4 register can also latch counter 1 or counter 2 in seven different ways.

1. When trigger signal to LTCn terminal is ON
2. When trigger signal to ORGn terminal is ON
3. When trigger signal to EZn terminal is ON
4. When trigger signal to P4n terminal is ON
5. When trigger signal to P5n terminal is ON
6. When trigger signal to P6n terminal is ON
7. When trigger signal to P7n terminal is ON

The input specification and latch timing can be selected with RENV4 register.

Event interrupt (RIST.ISL3) can be generated when trigger signal is ON and RCUN 1 register value is latched to RLTC3 register.

Event interrupt (RIST.ISL3) can also be generated when RCUN 2 register value is latched to RLTC3 register.

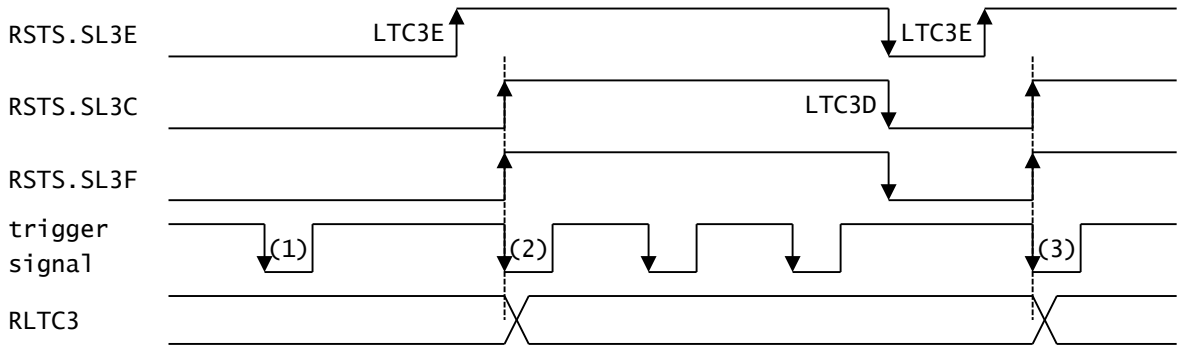
Event interrupt (RIST.ISL4) can be generated when trigger signal is ON and RCUN 1 register value is latched to RLTC4 register.

Event interrupt (RIST.ISL4) can also be generated when RCUN 2 register value is latched to RLTC4 register.

In operation example 1: Selects a value other than “invalid” (RENV4.L3T ≠ 000b) as the trigger signal of RLTC3 register and selects “RENV4.L3MD = 0” (latched only with the first trigger signal) as the latch operation specification.

<Operation Example 1>

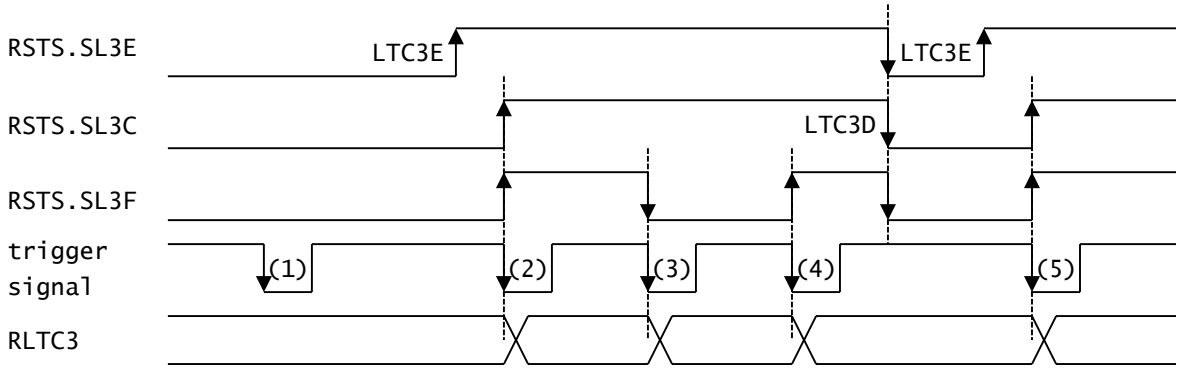
1. Before writing LTC3E (3Ch) command, the trigger signal is ON but will not latch. (1)
   RSTS.SL3C bit and RSTS.SL3F bit also do not change.
2. Start monitoring the trigger signal by writing LTC3E (3Ch) command.
3. After writing LTC3E (3Ch) command, the trigger signal is ON and latched. (2)
   RSTS.SL3C bit and RSTS.SL3F bit change.
4. No latch trigger signal from the second time on.
   RSTS.SL3C bit and RSTS.SL3F bit also do not change.
5. By writing LTC3D (3Eh) command, monitoring of trigger signals is terminated.
   Clear RSTS.SL3C bit and RSTS.SL3F bit.
6. When writing LTC3E (3Ch) command again, monitoring of trigger signals is resumed.
7. After writing the LTC3E (3Ch) command, the trigger signal is ON and latched. (3)
   RSTS.SL3C bit and RSTS.SL3F bit change.



Operation example 2: Selecting a value other than “invalid” (RENV4.L3T ≠ 000b) as the trigger signal of RLTC3 register and selecting “RENV4.L3MD = 1” (latched with every trigger signal) as latch operation specification.

<Operation Example 2>

1. Before writing LTC3E (3Ch) command, the trigger signal is ON but will not latch. (1)
   RSTS.SL3C bit and RSTS.SL3F bit also do not change.
2. Start monitoring trigger signals by writing LTC3E (3Ch) command.
3. After writing LTC3E (3Ch) command, the trigger signal is ON and latches. (2)
   RSTS.SL3C bit and RSTS.SL3F bit change.
4. Latch the second trigger signal ON (3)
   RSTS.SL3C bit does not change.
   RSTS.SL3F bit performs toggle changes.
5. Latch trigger signals ON will be latched from this time on. (4)
   RSTS.SL3C bit does not change.
   RSTS.SL3F bit performs toggle changes.
6. By writing LTC3D (3Eh) command, monitoring of trigger signals is terminated.
   Clear RSTS.SL3C bit and RSTS.SL3F bit.
7. When writing LTC3E (3Ch) command again, monitoring of trigger signals is resumed.
8. After writing the LTC3E (3Ch) command, the trigger signal is ON and latched. (5)
   RSTS.SL3C bit and RSTS.SL3F bit change.



Counter to latch to RLTC3 register <RENV4.L3DT(4)> 0: Select Counter 1 (RCUN1). 1: Select Counter 2 (RCUN2).	[RENV4] (R/W) 7 0 - - - n - - - -
Input terminal for the trigger signal latched to RLTC3 register <RENV4.L3T(2 to 0)> 000: Invalid 001: LTCn terminal 010: ORGn terminal 011: EZn terminal 100: P4n terminal 101: P5n terminal 110: P6n terminal 111: P7n terminal	[RENV4] (R/W) 7 0 - - - - - n n n
Input specification for the trigger signal to latch to RLTC3 register <RENV4.L3TL(3)> 0: Falling edge 1: Rising edge	[RENV4] (R/W) 7 0 - - - - n - - -
Latching specification of RLTC3 register. <RENV4.L3MD(5)> 0: Latched only by the 1st trigger signal. 1: Latched by every trigger signal.	[RENV4] (R/W) 7 0 - - n - - - - -
Input noise filter characteristics of trigger signal latched to RLTC3 register <RENV4.L3F(7, 6)> 00b: Recognizes signals with pulse width of 0.1 µs or wider. 01b: Recognizes signals with pulse width of 3.2 µs or wider. 10b: Recognizes signals with pulse width of 25 µs or wider. 11b: Recognizes signals with pulse width of 200 µs or wider. In addition, it does not affect the setting of RENV1.FLTR bit or RENV2.EINF bit.	[RENV4] (R/W) 7 0 n n - - - - - -
Monitoring status of trigger signal for RLTC3 register latching <RSTS.SL3E(17)> 0: Not monitor the trigger signal for RLTC3 register latching. 1: Monitor the trigger signal for RLTC3 register latching.	[RSTS] (R) 23 16 0 - - - - - n -
Monitoring status of trigger signal for RLTC3 register latching <RSTS.SL3C(18)> 0: Not latched by RLTC3 register. 1: Latched equal to or more than once by RLTC3 register.	[RSTS] (R) 23 16 0 - - - - n - -
Changes or not change of RLTC3 register. <RSTS.SL3F(Bit19)> Each time RLTC3 register value is changed, it toggles to change	[RSTS] (R) 23 16 0 - - - n - - -
Starts monitoring of trigger signals. (RLTC3) <LTC3E> Starts monitoring trigger signals for RLTC3 register latching.	[Command] 3Ch
Ends monitoring of trigger signal (RLTC3) <LTC3D> Ends monitoring trigger signals for RLTC3 register latching.	[Command] 3Eh
Counter to latch to RLTC4 register. <RENV4.L4DT(12)> 0: Select Counter 1 (RCUN1). 1: Select Counter 2 (RCUN2).	[RENV4] (R/W) 15 8 - - - n - - - -

Input terminal for the trigger signal latched to RLTC4 register <RENV4.L4T(10 to 8)> 000: Invalid 00: LTCn terminal 010: ORGn terminal 011: EZn terminal 100: P4n terminal 101: P5n terminal 110: P6n terminal 111: P7n terminal	[RENV4] (R/W) 15 8 - - - - - n n n
Input specification for the trigger signal latched to RLTC4 register <RENV4.L4TL(11)> 0: Falling edge 1: Rising edge	[RENV4] (R/W) 15 8 - - - - n - - -
Latching specification of RLTC4 register. <RENV4.L4MD(13)> 0: Latched only by the 1st trigger signal. 1: Latched by every trigger signal.	[RENV4] (R/W) 15 8 - - n - - - - -
Input noise filter characteristics of trigger signal latched to RLTC4 register <RENV4.L4F(15, 14)> 00b: Recognizes signals with pulse width of 0.1 µs or wider. 01b: Recognizes signals with pulse width of 3.2 µs or wider. 10b: Recognizes signals with pulse width of 25 µs or wider. 11b: Recognizes signals with pulse width of 200 µs or wider. In addition, it does not affect the setting of RENV1.FLTR bit or RENV2.EINF bit.	[RENV4] (R/W) 15 8 n n - - - - - -
Monitoring status of trigger signal for RLTC4 register latching <RSTS.SL4E(20)> 0: Not monitor the trigger signal for RLTC4 register latching. 1: Monitors the trigger signal for RLTC4 register latching.	[RSTS] (R) 23 16 0 - - n - - - -
Monitoring status of trigger signal for RLTC4 register latching <RSTS.SL4C(21)> 0: Not latched by RLTC4 register. 1: Latched equal to or more than once by RLTC4 register.	[RSTS] (R) 23 16 0 - n - - - - -
Changes or not change of RLTC4 register. <RSTS.SL4F(22)> Each time RLTC4 register value is changed, it toggles to change	[RSTS] (R) 23 16 0 n - - - - - -
Starts monitoring of trigger signals. (RLTC4) <LTC4E> Starts monitoring trigger signals for RLTC4 register latching.	[Command] 3Dh
Ends monitoring of trigger signal(RLTC4) <LTC4D> Ends monitoring trigger signals for RLTC4 register latching.	[Command] 3Fh

7.10.3 Counting stops and input stops

Counters 1 and 2 have counting stop (RENV3.CU1H, RENV3.CU2H) and input stop (PRMD.MCCE, RENV2.EOFF).

Counter 1 (RCUN1) and Counter 2 (RCUN2) can be stopped separately when counting is stopped.

When counting input is stopped, the counter that selects the corresponding input will stop.

In the operation mode of timer (RMD.MOD = 47h), the counter that has selected the command position to count will stop. The counter that has selected the machine position as the count target reflects a count stop and an input stop.

If you select command position as the count target and select “RENV1.PMSK = 1” (stop to output command pulses), command pulses are not output. If stopping to count is not selected, the counter counts.

Count of COUNTER 1(RCUN1) 0: Count the counting target 1: Not count.	<RENV3.CU1H(2)>	[RENV3] (R/W) 7 0 - - - - - n - -
Count of COUNTER 2(RCUN2) 0: Count the counting target. 1: Not count.	<RENV3.CU2H(3)>	[RENV3] (R/W) 7 0 - - - - n - - -
Count the command pulse 0: Count the command pulse. 1: Not count.	<PRMD.MCCE(11)>	[PRMD] (R/W) 15 8 - - - - n - - -
Input encoder signals.(EAn and EBn) 0: Encoder signal input is enabled. 1: Encoder signal input is disabled.	<RENV2.EOFF(14)>	[RENV2] (R/W) 15 8 - n - - - - - -
Command pulse output 0: Command pulse is output. 1: Command pulse is not output.	<RENV1.PMSK(31)>	[RENV1] (R/W) 31 24 n - - - - - - -

7.11 Comparators

7.11.1 Comparator types and functions

The LSI has four built-in 32-bit comparators per axis.

Comparator 1: Compares the setting value in the Comparator 1 (RCMP1) with Counter 1 (RCUN1).

Comparator 2: Compares the setting value in the Comparator 2 (RCMP2) with Counter 2 (RCUN2).

Comparator 3 and 4 are used only for software limit functions.

As for how to use comparators 3 and 4, see “7.11.3 Software limit function”.

Comparison conditions (RENV3.C1S, RENV3.C2S) of comparators 1 and 2 can be selected from three types (“=”, “>”, “<”).

Comparison results can be output from CP1 terminal and CP2 terminal.

Event interrupt (RIST.ISC1, RIST.ISC2) can be generated when the comparison conditions are met.

Comparators 1 and 2 can also be used for Ring count function and Synchronous start function.

For the explanation of Ring count function, see “7.11.2 Ring count function”.

For the explanation of Synchronous start function, please refer to “7.12.2 Start by internal synchronous signal”.

Comparison condition for Comparator 1 <RENV3.C1S(13, 12)> 00b: Does not use Comparator 1 01b: Selects “RCMP 1 register value = RCUN 1 register value”. 10b: Selects “RCMP 1 register value > RCUN 1 register value”. 11b: Selects “RCMP 1 register value < RCUN 1 register value”.	[RENV3] (R/W) 15 8 - - n n - - - -
Comparison condition for Comparator 2 <RENV3.C2S(15, 14)> 00b: Does not use Comparator 2 01b: Selects “RCMP 2 register value = RCUN 2 register value”. 10b: Selects “RCMP 2 register value > RCUN 2 register value”. 11b: Selects “RCMP 2 register value < RCUN 2 register value”.	[RENV3] (R/W) 15 8 n n - - - - - -
Sets Event interrupt factor <RIRQ.IRC1(6)> 1: Interrupt is generated when the condition of Comparator 1 is met.	[RIRQ] (R/W) 7 0 - n - - - - - -
Sets Event interrupt factor <RIRQ.IRC2(7)> 1: Interrupt is generated when the condition of Comparator 2 is met.	[RIRQ] (R/W) 7 0 n - - - - - - -
Obtains Event interrupt factor <RIST.ISC1(6)> 1: Condition of Comparator 1 is met.	[RIST] (R/W) 7 0 - n - - - - - -

Obtains Event interrupt factor <RIST.ISC2(7)> 1: Condition of Comparator 2 is met.	[RIST] (R/W) 7 0 n - - - - - - -
Obtains Comparator 1 status <MSTS.SCP1(8)> 0: Condition of Comparator 1 is not met. 1: Condition of Comparator 1 is met.	[MSTS] (R) 15 8 - - - - - - - n
Obtains Comparator 2 status <MSTS.SCP2(9)> 0: Condition of Comparator 2 is not met. 1: Condition of Comparator 2 is met.	[MSTS] (R) 15 8 - - - - - - n -
Function specification of P3/CP1 terminal <RENV2.P3M(7, 6)> 00b: General-purpose input 01b: General-purpose output 10b: Negative logic output of CP1(condition of Comparator 1 is met) 11b: Positive logic output of CP1(condition of Comparator 1 is met)	[RENV2] (R/W) 7 0 n n - - - - - -
Function specification of P4/CP2 terminal <RENV2.P4M(9, 8)> 00b: General-purpose input 01b: General-purpose output 10b: Negative logic output of CP2 (condition of Comparator 2 is met) 11b: Positive logic output of CP2 (condition of Comparator 2 is met)	[RENV2] (R/W) 15 8 - - - - - - n n

7.11.2 Ring count function

COUNTER 1 and COUNTER 2 can be set for Ring count function to control a rotating table.

When using the Ring count function, set positive numbers to RCMP1 register and RCMP2 register.

When “RENV3.C1RM = 1” (Ring counter) is set in COUNTER 1 (RCUN1), the LSI can perform the following operations:

- Count value will be “0” when the counter counts up from the “set value in RCMP1 register”.
- Count value will be equal to the set value in RCMP1 register when the counter counts down from “0”.

When “RENV3.C2RM = 1” (Ring counter) is set in COUNTER 2 (RCUN2), the LSI can perform the following operations:

- Count value will be “0” when the counter counts up from the “set value in RCMP2 register”.
- Count value will be equal to the set value in RCMP2 register when the counter counts down from “0”

Ring counter for COUNTER 1 (RCUN1) 0: Not operate the ring counter using Comparator 1. 1: Operate the ring counter using comparator 1.	<RENV3.C1RM(7)>	[RENV3] (R/W) 7 0 n - - - - - - -
Ring counter for COUNTER 2 (RCUN2) 0: Not operate the ring counter using Comparator 2. 1: Operate the ring counter using comparator 2.	<RENV3.C2RM(11)>	[RENV3] (R/W) 15 8 - - - - n - - -

The feeding amount (PRMV) for positioning control can be out of the range of “0” to “comparator comparison value (RCMP1, 2)”. For example, if you set “RCUN1 = 0”, “RCMP1 = 3599”, “RENV3 = 80h”, “PRMD.MOD = 41h”, “PRMV = 7200” for a rotating table of 3600 pulses per rotation, the table rotates 2 times and RCUN1 becomes 0 (“RCUN1=0”).

Note: Change the counter value from “0” to the value within the range of “RCMPn register setting” before setting it as the Ring counters. If the counter value is out of the range, it will not operate properly.

To use COUNTER 1 (RCUN1) as Ring counter, set it to “RENV3.C1S = 00b”.

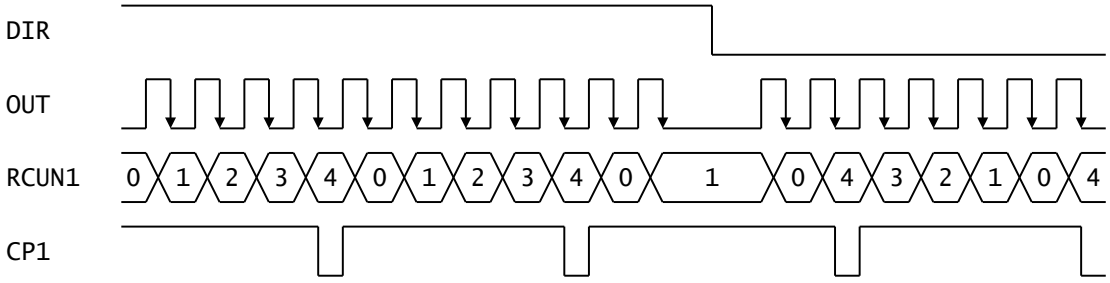
To use COUNTER 2 (RCUN2) as Ring counter, set it to “RENV3.C2S = 00b”.

[Setting example]

RCUN1 = 0 ……Clear COUNTER 1 (RCUN1) to “0”.

RCMP1 = 4 ……Counting range is 0 to 4.

RENV3 = 00000080h ……COUNTER 1(RCUN1) is used for a Ring counter operation (RENV3.C1RM = 1)
Comparator 1 is not used.(RENV3.C1S = 00b)



7.11.3 Software limit function

In addition to hardware limit switch controls by positive or negative direction signal, software limit controls can be used.

Comparator 3 comparison value (RCMP 3) is the positive direction software limit value (PSL).

Comparator 4 comparison value (RCMP 4) is the negative direction software limit value (MSL).

Counters for software limit managements can be selected (RENV3.SLCU) from COUNTER 1 (RCUN1) and COUNTER 2 (RCUN2).

By comparing the selected counter value with the software limit value, an event or error interrupt can be generated.

An event interrupt can be generated by selecting “RENV3.SLM = 01b” for Software limit function.

A positive direction event interrupt (RIST.ISPS) is generated when the selected counter value exceeds PSL (RCMP 3).

An event interrupt (RIST.ISMS) in negative side is generated when the selected counter value is less than MSL (RCMP4).

Even if an event interrupt occurs, operation will not stop.

An error interrupt can be generated by selecting “RENV3.SLM = 10b” or “RENV3.SLM = 11b” for Software limit function.

A positive direction error interrupt (REST.ESPS) is generated when the selected counter value exceeds PSL (RCMP3).

An error interrupt (REST.ESMS) in negative direction is generated when the selected counter value is less than MSL (RCMP 4).

When an error interrupt is generated, the operation stops immediately if "RENV3.SLM = 10b"; the operation decelerates and stops if “RENV3.SLM = 11b”.

In the case of FL constant speed start or FH constant speed start, the operation stops immediately.

The status of Software limit can be checked with Main-status (MSTS.SCP3, MSTS.SCP4).

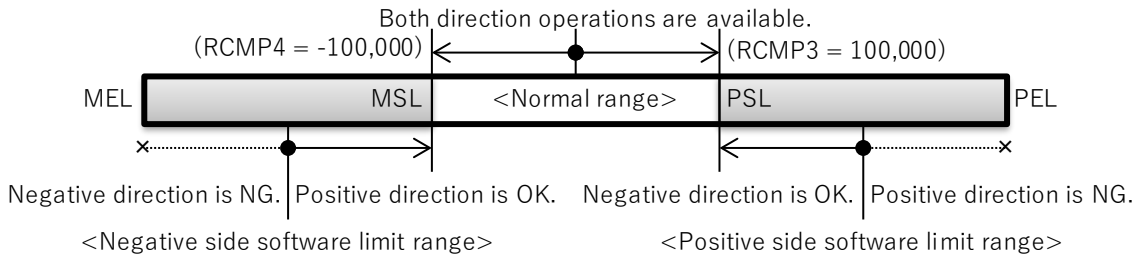
It is not related to the selection of software limit function (RENV3.SLM).

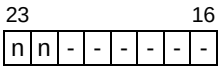
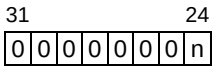
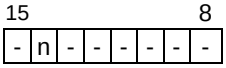
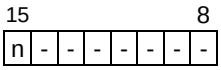
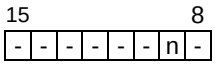
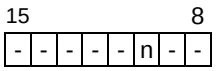
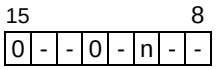
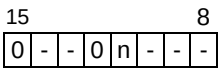
“MSTS.SCP 3 = 1” when the selected counter value is more than PSL (RCMP 3).

“MSTS.SCP 4 = 1” when the selected counter value is less than MSL (RCMP 4).

[Setting example]

RENV3 = 00C0000h:	Select counter 1 (RCUN 1) for Software limit management counter (RENV 3.SLCU = 0)
	Select deceleration stop by error interrupt (RENV3.SLM = 11b) for Software limit function.
RCMP3 = 100,000:	Positive direction Software limit value (PSL)
RCMP4 = -100,000:	Negative direction Software limit value (MSL)



Software limit function <RENV3.SLM(23, 22)> 00b: Operation does not stop at software limit positions, and no interrupt is generated. 01b: Operation does not stop at software limit positions, and an event interrupt is generated. 10b: Operation stops immediately at software limit positions, and an error interrupt is generated. 11b: Operation decelerates and stops at software limit positions, and an error interrupt is generated.	[RENV3] (R/W) 
Selection of Software limit control counter. <RENV3.SLCU(24)> 0: Selects COUNTER 1 (RCUN1). 1: Selects COUNTER 2 (RCUN2).	[RENV3] (R/W) 
Obtains Event interrupt factor. <RIST.ISPS(14)> 1: Software limit signal in positive direction is detected. Event interrupt is generated when “RENV3.SLM = 01b”.	[RIST] (R/W) 
Obtains Event interrupt factor. <RIST.ISMS(15)> 1: Software limit signal in negative direction is detected. Event interrupt is generated when “RENV3.SLM = 01b”.	[RIST] (R/W) 
Obtains Error interrupt factor. <REST.ESPS(9)> 1: Operation is stopped by positive direction software limit signal detection. Error interrupt is generated when “RENV3.SLM = 10b” and “RENV3.SLM = 11b”.	[REST] (R/W) 
Obtains Error interrupt factor. <REST.ESMS(10)> 1: Operation is stopped by negative direction software limit signal detection. Error interrupt is generated when “RENV3.SLM = 10b” and “RENV3.SLM = 11b”.	[REST] (R/W) 
Obtains Software limit status. <MSTS.SCP3(10)> 0: Software limit management counter value is equal to or less than RCMP3 register value. 1: Software limit management counter value exceeds RCMP3 register value. Comparison result monitor of comparator for software limit detection for positive direction.	[MSTS] (R) 
Obtain Software limit status. <MSTS.SCP4(11)> 0: Software limit management counter value is equal to or more than RCMP4 register value. 1: Software limit management counter value is less than RCMP4 register value. Comparison result monitor of comparator for software limit detection for negative direction.	[MSTS] (R) 

7.12 Synchronous starting

There are two types of start that synchronize with the movements of other axes.

7.12.1 Starts by stopping the target axis

When “PRMD.MSY = 11b” is selected for start timing and then start, RSTS.CND becomes 0100b.

After that, when any target axis (RMD.MAX) starts and the all target axes stop, the own-axis will start.

Start timing <PRMD.MSY(19, 18)> 11b: Operation will start when the target axis (RMD.MAX) stops.	[PRMD] (R/W) 23 16 - - - - n n - -
Selects the target axis to check stopping. <PRMD.MAX3 to 0(23 to 20)> In case of “RMD.MSY = 11b”, selects the target axis to check stopping. MAX0 = 1: X-axis MAX1 = 1: Y-axis MAX2 = 1: Z-axis MAX3 =1: U-axis	[PRMD] (R/W) 23 16 n n n n - - - -
Obtains the motion status <RSTS.CND(3 to 0)> 0011b: Wait for stop of the target axis.	[RSTS] (R) 7 0 - - - - n n n n

[Setting example]

(1) Sets “PRMD.MSY = 11b” on U-axis. (Starts when the target axis stops)

(2) Sets “PRMD.MAX = 0011b” on U-axis. (When both X and Y axes stop)

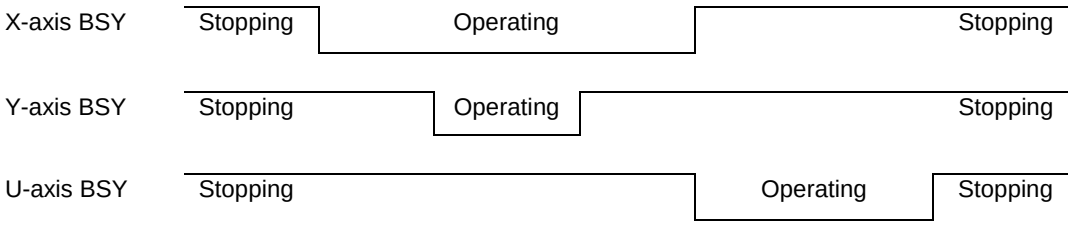
(3) Writes a start command to U-axis. (U-axis will not start.)

(4) Writes a start command to X-axis. (X-axis will start.)

(5) Writes a start command to Y-axis. (Y-axis will start.)

(6) After both X and Y axes stop, U-axis will start.

[Operation example]



If any one of target axes starts and then stops, the own-axis will start even if the remaining target axes do not start and remain stopped.

In the above [Setting example], U-axis starts by X-axis stopping even though Y-axis has not started before X-axis stops.

7.12.2 Start by internal synchronous signal

When “PRMD.MSY = 10b” is selected for start timing and then start, RSTS.CND becomes “0011b”.

After that, when an internal synchronous signal is output from the target axis (RENV3.SYI), the own-axis starts.

There are 6 types of output condition (RENV3.SYO) for the internal synchronous signal.

Event interrupts (RIST.ISUS, ISUE, ISDS, ISDE, ISC1, and ISC2) related to output conditions can be generated.

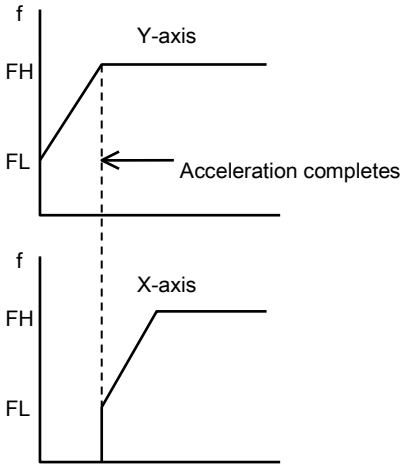
Start timing <PRMD.MSY(19, 18)> 10b: Start with internal synchronous signal (RENV3.SYI).	[PRMD] (R/W) 23 16 - - - - n n - -
Output condition of internal synchronous signal. <RENV3.SYO(19 to 16)> 0001b: Comparator 1 condition is met. 0010b: Comparator 2 condition is met. 1000b: When acceleration starts. 1001b: When acceleration ends. 1010b: When deceleration starts. 1011b: When deceleration ends. Other: Internal synchronization signal is not output.	[RENV3] (R/W) 23 16 - - - - n n n n
Target of input of internal synchronization signal <RENV3.SYI(21, 20)> 00b: Internal synchronous signal output by X-axis. 01b: Internal synchronous signal output by Y-axis. 10b: Internal synchronous signal output by Z-axis. 11b: Internal synchronous signal output by U-axis.	[RENV3] (R/W) 23 16 - - n n - - - -
Obtains the operation status. <RSTS.CND(3 to 0)> 0011b: Wait for the input of internal synchronous signal.	[RSTS] (R) 7 0 - - - - n n n n

The following Setting example 1 shows to use an acceleration completion as the internal synchronous signal.

[Setting example 1]

After setting steps 1) to 3) below, write start commands to both X- and Y-axes so that Y-axis will start. When the acceleration of Y-axis completes, X-axis will start.

1) Set “PRMD.MSY = 10b” (Internal synchronous signal) as the start timing of X-axis.
2) Set “RENV3.SYI = 01b” (Y-axis) as the input target of X-axis.
3) Set “RENV3.SYO=1001b” (Acceleration completes) as the output condition of Y-axis.



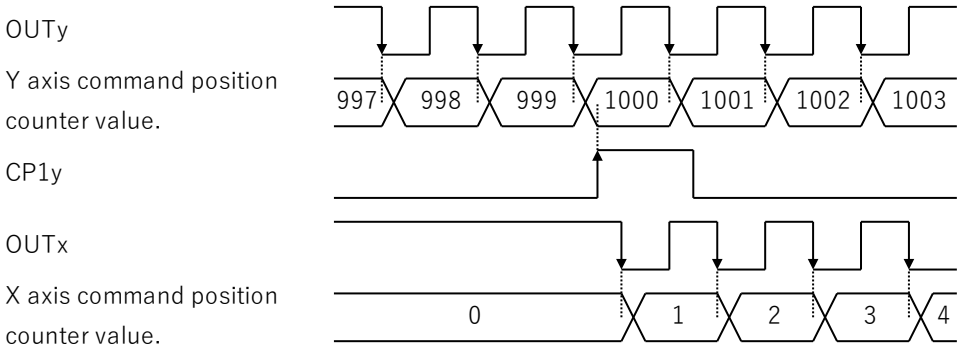
The following Setting example 2 shows to use a fulfillment of comparator condition as the internal synchronization signal.

[Setting Example 2]

After setting step 1) to 5) below, write start commands to both X- and Y-axes so that Y-axis will start.

When the counter 1 (RCUN1) of Y-axis matches “1000” of the comparator 1 comparison value (RCMP1), X-axis will start:

1) Sets “PRMD.MSY = 10b” (internal synchronous signal) for X-axis start timing.
2) Sets “RENV3.SYI = 01b” (Y-axis) as the input target of X-axis.
3) Sets “RENV3.SYO = 0001b” (Comparator 1 is met) as the output condition of Y-axis.
4) Sets “RENV3.C1S = 01b” (“RCMP1 register value = RCUN1 register value”) as the comparison condition of Comparator 1 of Y-axis.
5) Sets “RCMP1 = 1000” (1000) to the comparison value of Comparator 1 of Y-axis.



Note: In the example above, if you set “PRMVy = 2000” and “PRMVx = 1000”, it becomes “RCUN1x = 1” when “RCUN1y = 1000”.

Therefore, it becomes “RCUN1x = 1000”, when “RCUN1y = 1999”, so that X-axis stops 1 pulse before Y-axis.

If you want “RCUN1 x = 1000” when “RCUN1y = 2000”, be sure to set the Comparator 1 comparison condition to “RENV3.C1S = 11b” (“RCMP 1 register value < RCUN 1 register value”) or “RCMP1y = 1001”.

7.13 Interrupt (INT) function

This LSI can output an interrupt requesting signal (INT = L level) from INT terminal.

Interrupt signal is output triggered by 11 types of errors, 20 types of events, and 1 type of change from operating to stop; totaling 32 types. “INT = L level” is output unconditionally if it is triggered by error interrupt factors.

If it is triggered by event interrupt factors, it becomes INT = L level under the condition set in RIRQ or RENV3 registers. If it is triggered by stop interrupt factors, it becomes INT = L level under the condition set in RENV2.IEND bit.

There is no distinction between normal stops and abnormal stops in terms of stop interrupt factors.

Normal stop interrupts are also included in the event interrupt factors but read processing of RIST register is required.

If it is not necessary to distinguish between normal stop and abnormal stop, stop interrupt (MSTS.SENI) can be used

Interrupt request signal continues to be output until all the factors of the entire axes that are generating interrupts are cleared.

The timing of clearing the interrupt factor is shown in the following table.

Interrupt factor	If “RENV2.MRST = 0” (Automatic clear by reading)	If “RENV2.MRST = 1” (Manual clear by reading)
REST register	When writing RREST (F2h) command	When writing WREST (B2h) command
RIST register	When writing RRIST (F3h) command	When writing WRIST (B3h) command
MSTS.SENI bit	When reading the main-status (MSTS)	When writing SENIR (2Dh) command

To determine the axis and type of interrupt occurred, follow the procedures below:

1) Read the main-status of X-axis and check whether bit 2, 4, or 5 is “1”.
2) If “MSTS.SENI = 1” (bit 2), a stop interrupt has occurred.

   When “RENV2.MRST = 1”, execute SENIR (2Dh) command and clear the corresponding bit.
3) If “MSTS.SERR = 1” (bit 4), read REST to identify the error interrupt factor.

   When “RENV2.MRST = 1”, execute WREST (B2h) command, write “1” to the corresponding bit, and clear.

   If “MSTS.SINT = 1” (bit 5), read RIST to identify the event interrupt factor.

   When “RENV2.MRST = 1”, execute WRIST (B3h) command, write “1” to the corresponding bit, and clear.
5) Repeat the steps 1) to 4) above for the rest of axes.

By the above procedure, determine the interrupt factors and reset “INT = H level”.

Note:

1. In parallel bus interface, reading the register with the interrupt routine will change the contents of I/O buffer.
   Since the I/O buffers are common, when the interrupt routine by “INT = L level” is activated during the register reading and writing in the main routine, it affects the processing of the main routine.
   In the interrupt routine, take countermeasures for exclusive control such as reading the contents of I/O buffer first and then writing the original contents after interrupt processing.

2: While processing all axes in steps 1) to 4) above, it is possible that another interrupt may occur on the axis whose process has completed. When the CPU interrupt reception mode is set to edge triggering, the new interrupt will not be accepted. Read the main-status of all axes again and check “INT = H level” before exiting the interrupt routine is completed.

3: When not using INT terminal, leave it opens. Even if multiple LSIs are used, INT terminals cannot be connected with each other by wired-OR connection. (INT≠ Hi-z)

Outputs of interrupt requesting signals can be stopped with “RENV1.INTM = 1”.

When an interrupt request signal output is stopped, it will not change to “INT = L level” when an interrupt occurs.

Main-status and interrupt factor register can change.

When “RENV1.INTM = 0” is set while interrupt is occurring, INT changes to L level (“INT=L level”).

Obtains the interrupt status <MSTS.SINT(5), MSTS.SERR(4), MSTS.SENI(2)> SENI = 1: Stop interrupt occurred. SERR = 1: Error interrupt occurred. SINT = 1: Event interrupt occurred.	[MSTS] (R) 7 0 - - n n - n - -
Outputs the interrupt requesting signal <RENV1.INTM(29)> 0: “INT = L level” is output when an interrupt occurs. 1: “INT = L level” is not output when an interrupt occurs. Main-status and interrupt factor register will change.	[RENV1] (R/W) 31 24 - - n - - - - -
Stop interrupt (MSTS.SEND) <RENV2.IEND(30)> 0: Stop interrupt will not occur. 1: Stop interrupt will occur. It becomes “INT = L level” when stopped regardless of normal stop or abnormal stop.	[RENV2] (R/W) 31 24 - n - - - - - -
How to reset interrupt factors. <RENV2.MRST(31)> 0: Automatic clear by reading. 1: Manual clear by writing.	[RENV2] (R/W) 31 24 n - - - - - - -
Obtains the error interrupt factor. <RREST> Read out REST register value to I/O buffer.	[Command] F2h
Obtains the event interrupt factor <RRIST> Read out RIST register value to I/O buffer.	[Command] F3h
Sets the event interrupt factor. <WRIRQ> Writes I/O buffer data into RIRQ register.	[Command] ACh
Clears the error interrupt factor. <WREST> Writes I/O buffer data into REST register.	[Command] B2h
Clears the event interrupt factor. <WRIST> Writes I/O buffer data into RIST register.	[Write command] B3h
Clears the stop interrupt. <SENIR> Clears MSTS.SENI bit (stop interrupt).	[Command] 2Dh

7.13.1 Error interrupt factors

Error interrupt factors <Interrupt factor occurs when the corresponding bit is “1”.>	REST	
	Position	Name
Stopped by positive direction end limit signal turned ON.	0	ESPL
Stopped by negative direction end limit signal turned ON.	1	ESML
Stopped by alarm signal ON, or alarm signal turned ON while stopping.	2	ESAL
Stopped by Simultaneous stop signal turned ON.	3	ESSP
Emergency stop signal turns ON or write CEMEMG (05h) command.	4	ESEM
Stopped by slow-down signal turned ON.	5	ESSD
Stopped due to the overflow at buffer counter with manual pulser signals.	6	ESPO
Encoder signal input error occurred.	7	ESEE
Input error of manual pulser signal occurred.	8	ESPE
Stopped by detecting the software limit on the positive side.	9	ESPS
Stopped by detecting the software limit on the negative side.	10	ESMS

7.13.2 Event interrupt factors

Event interrupt factors <When an interrupt factor is set and is occurred, the corresponding bit becomes “1”.>	RIRQ		RIST	
	Position	Name	Position	Name
Stopped normally.	0	IREN	0	ISEN
Pre-register changed to write enabled.	1	IRNM	1	ISNM
Acceleration started.	2	IRUS	2	ISUS
Acceleration ended.	3	IRUE	3	ISUE
Deceleration started.	4	IRDS	4	ISDS
Deceleration ended.	5	IRDE	5	ISDE
Comparator 1 condition was met.	6	IRC1	6	ISC1
Comparator 2 condition was met.	7	IRC2	7	ISC2
The counter value was latched by input of counter latch signal.	8	IRLT	8	ISLT
Origin positon signal turned ON.	9	IROL	9	ISOL
Slow-down signal turned ON.	10	IRSD	10	ISSD
Input of positive direction switch signal changed.	11	IRDR	11	ISPD
Input of negative direction switch signal changed.			12	ISMD
Changed to “CSTA = L level”.	12	IRSA	13	ISSA
Software limit on positive direction was detected.	-	-	14	ISPS
Software limit on negative direction was detected.	-	-	15	ISMS
Stopped during deceleration with “RENV2.ORM = 1”.	13	IREZ	16	ISEZ
Started.	14	IRBY	17	ISBY
Count value was latched in RLTC3 register.	16	IRL3	18	ISL3
Count value was latched in RLTC4 register.	17	IRL4	19	ISL4

7.14 ID Monitor

The LSIs in this series have ID codes in order to distinguish them from other LSI products.

ID codes can be checked with the following procedures:

1. Write IDMON (03h) command to X-axis.
2. Write RRMG (D5h) command to X- axis.
3. Read I/O buffer of X-axis.
4. Check the upper 16-bits of the read data.

ID codes can be read only when IDMON (03h) command and RRMG (D5h) command are used continuously. If RRMG (D5h) command is used other than the above procedure, the ID code part will be “0”.

The ID codes are as shown in the table below.

LSI	ID code
PCL6115	03E0h
PCL6125	03F0h
PCL6145	0400h

ID code <RMG.IDCD(31 to 16)> IDCD bit is in RMG register. ID code can be read only immediately after IDMON (03h) command is written. Usually “0” can be read. Writing to this bit is ignored.	[RMG] (R/W) 31 24 n n n n n n n n 23 16 n n n n n n n n
ID code confirmation command <IDMON> Sets ID code in the upper 16 bits of RMG register. The set ID code can be read only once with writing RRMG (D5h) command. It is cleared by writing commands other than IDMON (03h) command	[Command] 03h
Obtains RMG register <RRMG> Read out RMG register value to I/O buffer.	[Command] D5h

8. Electrical Characteristics

8.1 Absolute maximum ratings

Item	Name	Rating	Unit	Remark
Power supply voltage	V_{DD}	− 0.3 to + 4.0	V	-
Input voltage	V_{IN}	− 0.3 to + 7.0	V	-
Output current	I_{OUT}	− 30 to + 30	mA	-
Storage temperature	Tstg	− 65 to + 150	°C	-

8.2 Recommended operating conditions

Item	Name	Rating			Unit	Remark
		Min.	Typ.	Max.		
Power supply voltage	V_{DD}	3.0	3.3	3.6	V	-
Ambient temperature	T_J	−40	-	+85	°C	No condensation

8.3 DC characteristics

8.3.1 PCL6115

Item	Name	Condition	Min.	Max.	Unit
Consumption current	I_{dd1}	CLK = 30 MHz, 15 Mpps per axis, No load	-	37	mA
Input capacity	-	-	-	10	pF
L level input current (V_{IL} = GND)	I_{IL}	A0 to A2, D0 to D15, CLK	-1	-	uA
		Input terminals other than the above (Note)	-125	-	
H level input current	I_{IH}	$V_{IH} = V_{DD}$	-	1	uA
		V_{IH} = 5.5 V	-	30	
L level input voltage	V_{IL}	-	-0.3	0.8	V
H level input voltage	V_{IH}	-	2.0	5.8	V
L level output voltage	V_{OL}	I_{OL} = 6 mA	-	0.4	V
H level output voltage	V_{OH}	I_{OH} = -6 mA	V_{DD}-0.4	-	V
L level output current	I_{OL}	V_{OL} = 0.4 V	-	6	mA
H level output current	I_{OH}	$V_{OH} = V_{DD}$ -0.4 V	-6	-	mA
Internal pull up resistance	R_{PU}	Other than A0 to A2, D0 to D15 and CLK	40	240	k-ohm

Note: Internal pull up resistors are integrated for safety when they are open.

Signs of current values refer to current flow in with a positive value; flow out with a negative value.

8.3.2 PCL6125

Item	Name	Condition	Min.	Max.	Unit
Consumption current	I_{dd2}	CLK = 30 MHz, 2 axes at 15 Mpps, no load	-	75	mA
Input capacity	-	-	-	10	pF
L level input current (V_{IL} = GND)	I_{IL}	A0 to A3, D0 to D15, CLK	-1	-	uA
		Input terminals other than the above (Note)	-125	-	
H level input current	I_{IH}	$V_{IH} = V_{DD}$	-	1	uA
		V_{IH} = 5.5 V	-	30	
L level input voltage	V_{IL}	-	-0.3	0.8	V
H level input voltage	V_{IH}	-	2.0	5.8	V
L level output voltage	V_{OL}	I_{OL} = 6 mA	-	0.4	V
H level output voltage	V_{OH}	I_{OH} = -6 mA	V_{DD} -0.4	-	V
L level output current	I_{OL}	V_{OL} = 0.4 V	-	6	mA
H level output current	I_{OH}	$V_{OH} = V_{DD}$ −0.4 V	-6	-	mA
Internal pull up resistance	R_{PU}	Other than A0 to A3, D0 to D15, CLK	40	240	k-ohm

Note: Internal pull up resistors are integrated for safety when they are open.

Signs of current values refer to current flow in with a positive value; flow out with a negative value.

8.3.3 PCL6145

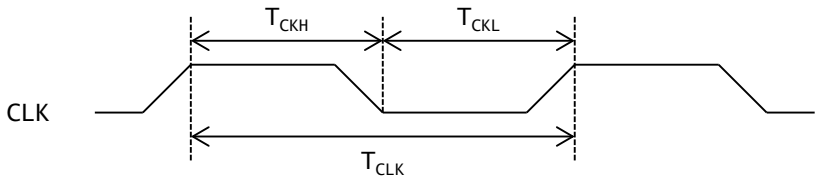
Item	Name	Condition	Min.	Max.	Unit
Consumption current	I_{dd4}	CLK = 30 MHz, 4 axes at 15 Mpps, no load	-	139	mA
Input capacity	-	-	-	10	pF
L level input current (V_{IL} = GND)	I_{IL}	A0 to A4, D0 to D15, CLK	−1	-	uA
		Input terminals other than the above (Note)	−125	-	
H level input current	I_{IH}	$V_{IH} = V_{DD}$	-	1	uA
		V_{IH} = 5.5 V	-	30	
L level input voltage	V_{IL}	-	−0.3	0.8	V
H level input voltage	V_{IH}	-	2.0	5.8	V
L level output voltage	V_{OL}	I_{OL} = 6 mA	-	0.4	V
H level output voltage	V_{OH}	I_{OH} = −6 mA	V_{DD} −0.4	-	V
L level output current	I_{OL}	V_{OL} = 0.4 V	-	6	mA
H level output current	I_{OH}	$V_{OH} = V_{DD}$ −0.4 V	−6	-	mA
Internal pull up resistance	R_{PU}	Other than A0 to A4, D0 to D15, CLK	40	240	k-ohm

Note: Internal pull up resistors are integrated for safety when they are open.

Signs of current values refer to current flow in with a positive value; flow out with a negative value.

8.4 AC characteristics

8.4.1 Reference Clock



8.4.1.1 PCL6115

Item	Name	Min.	Max.	Unit
Reference clock frequency	f_{CLK}	-	30	MHz
Reference clock cycle	T_{CLK}	33	-	ns
Reference clock H level width	T_{CKH}	13	-	ns
Reference clock L level width	T_{CKL}	13	-	ns

8.4.1.2 PCL6125

Item	Name	Min.	Max.	Unit
Reference clock frequency	f_{CLK}	-	30	MHz
Reference clock cycle	T_{CLK}	33	-	ns
Reference clock H level width	T_{CKH}	13	-	ns
Reference clock L level width	T_{CKL}	13	-	ns

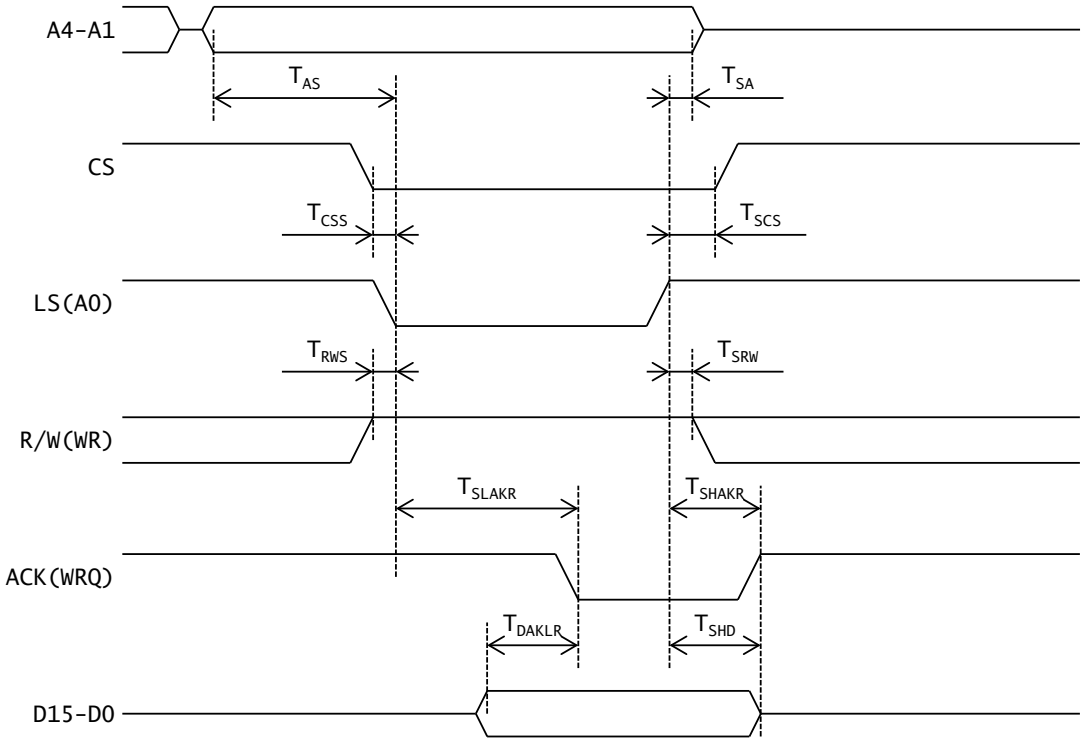
8.4.1.3 PCL6145

Item	Name	Min.	Max.	Unit
Reference clock frequency	f_{CLK}	-	30	MHz
Reference clock cycle	T_{CLK}	33	-	ns
Reference clock H level width	T_{CKH}	13	-	ns
Reference clock L level width	T_{CKL}	13	-	ns

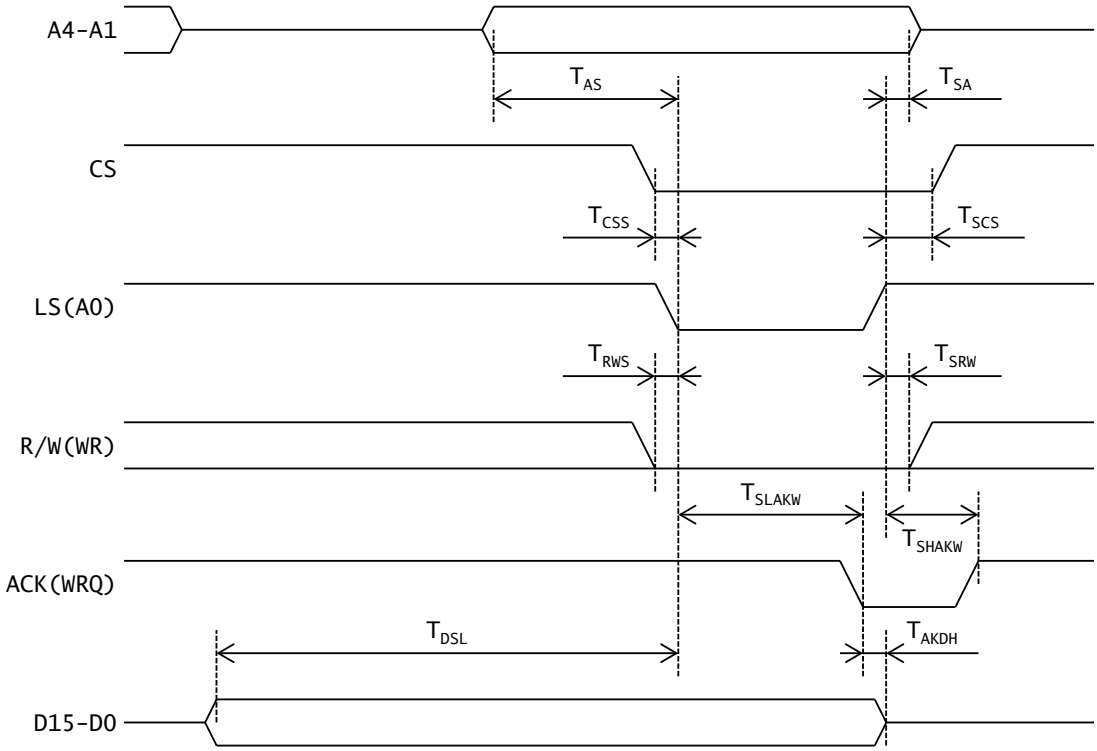
8.4.2 16-bit interface-1 (68000, etc.)

Setting: IF1 terminal = L level, IF0 terminal = L level.

<Read cycle>



<Write cycle>



8.4.2.1 PCL6115

Item		Name	Condition	Min.	Max.	Unit
Address setup time	for LS ↑	T_{AS}	-	11	-	ns
Address hold time	for LS ↑	T_{SA}	-	0	-	ns
CS setup time	for LS ↓	T_{CSS}	-	0	-	ns
CS hold time	for LS ↑	T_{SCS}	-	1	-	ns
R/W setup time	for LS ↓	T_{RWS}	-	0	-	ns
R/W hold time	for LS ↑	T_{SRW}	-	0	-	ns
ACK ON delay time	for LS ↓	T_{SLAKR}	C_L = 40pF	T_{CLK}	$4 \cdot T_{CLK}$ +12	ns
		T_{SLAKW}	C_L = 40pF	T_{CLK}	$4 \cdot T_{CLK}$ +12	ns
ACK OFF delay time	for LS ↑	T_{SHAKR}	C_L = 40pF	-	16	ns
		T_{SHAKW}	C_L = 40pF	-	16	ns
Data output prior time	for ACK ↓	T_{DAKLR}	C_L = 40pF	T_{CLK}	-	ns
Data float delay time	for LS ↑	T_{SHD}	C_L = 40 pF	-	21	ns
Data setup time	for LS ↓	T_{DSL}	-	14	-	ns
Data hold time	for ACK ↓	T_{AKDH}	-	0	-	ns

8.4.2.2 PCL6125

Item		Name	Condition	Min.	Max.	Unit
Address setup time	for LS ↓	T_{AS}	-	11	-	ns
Address hold time	for LS ↑	T_{SA}	-	0	-	ns
CS setup time	for LS ↓	T_{CSS}	-	1	-	ns
CS hold time	for LS ↑	T_{SCS}	-	0	-	ns
R/W setup time	for LS ↓	T_{RWS}	-	0	-	ns
R/W hold time	for LS ↑	T_{SRW}	-	0	-	ns
ACK ON delay time	for LS ↓	T_{SLAKR}	C_L = 40pF	T_{CLK}	$4 \cdot T_{CLK}$ +12	ns
		T_{SLAKW}	C_L = 40pF	T_{CLK}	$4 \cdot T_{CLK}$ +12	ns
ACK OFF delay time	for LS ↑	T_{SHAKR}	C_L = 40pF	-	16	ns
		T_{SHAKW}	C_L = 40pF	-	16	ns
Data output prior time	for ACK ↓	T_{DAKLR}	C_L = 40pF	T_{CLK}	-	ns
Data float delay time	for LS ↑	T_{SHD}	C_L = 40pF	-	21	ns
Data setup time	for LS ↓	T_{DSL}	-	16	-	ns
Data hold time	for ACK ↓	T_{AKDH}	-	0	-	ns

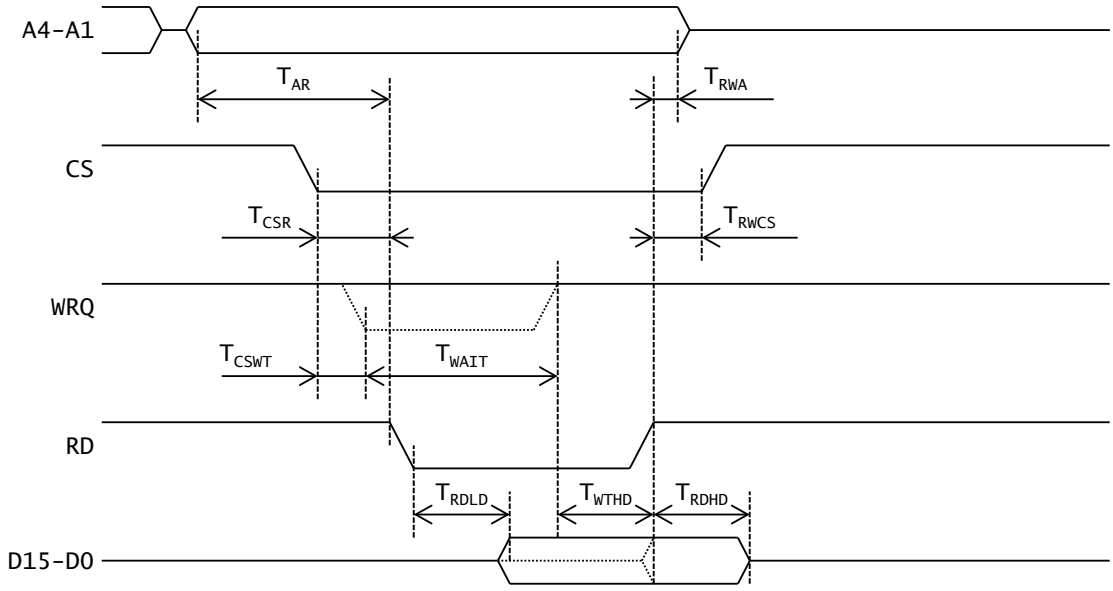
8.4.2.3 PCL6145

Item		Name	Condition	Min.	Max.	Unit
Address setup time	for LS ↓	T_{AS}	-	12	-	ns
Address hold time	for LS ↑	T_{SA}	-	0	-	ns
CS setup time	for LS ↓	T_{CSS}	-	1	-	ns
CS hold time	for LS ↑	T_{SCS}	-	0	-	ns
R/W setup time	for LS ↓	T_{RWS}	-	0	-	ns
R/W hold time	for LS ↑	T_{SRW}	-	1	-	ns
ACK ON delay time	for LS ↓	T_{SLAKR}	C_L = 40pF	T_{CLK}	$4 \cdot T_{CLK}$ +13	ns
		T_{SLAKW}	C_L = 40pF	T_{CLK}	$4 \cdot T_{CLK}$ +13	ns
ACK OFF delay time	for LS ↑	T_{SHAKR}	C_L = 40pF	-	17	ns
		T_{SHAKW}	C_L = 40pF	-	17	ns
Data output prior time	for ACK ↓	T_{DAKLR}	C_L = 40pF	T_{CLK}	-	ns
Data float delay time	for LS ↑	T_{SHD}	C_L = 40pF	-	23	ns
Data setup time	for LS ↓	T_{DSL}	-	17	-	ns
Data hold time	for ACK ↓	T_{AKDH}	-	0	-	ns

8.4.3 16-bit interface-2 (H8, etc.)

Setting: IF1 terminal = L level, IF0 terminal = H level

<Read cycle>



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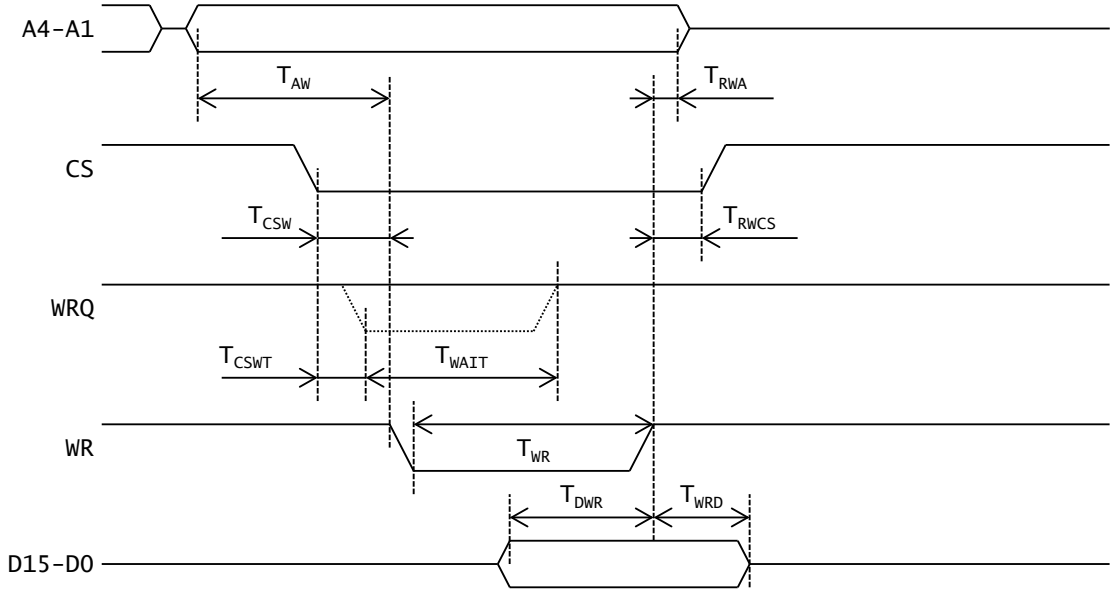


8.4.3.1 PCL6115

Item		Name	Condition	Min.	Max.	Unit
Address setup time	for RD ↓	T_{AR}	-	11	-	ns
Address setup time	for WR ↓	T_{AW}	-	0	-	ns
Address hold time	for RD, WR ↑	T_{RWA}	-	0	-	ns
CS setup time	for RD↓	T_{CSR}	-	0	-	ns
CS setup time	for WR ↓	T_{CSW}	-	0	-	ns
CS hold time	for RD, WR ↑	T_{RWCS}	-	0	-	ns
WRQ ON delay time	for CS↓	T_{CSWT}	C_L = 40pF	-	13	ns
WRQ signal L level time		T_{WAIT}	-	-	4･T_{CLK}	ns
Data output delay time	for RD ↓	T_{RDLD}	C_L = 40pF	-	13	ns
Data output delay time	for WRQ ↑	T_{WTHD}	C_L = 40pF	-	8	ns
Data float delay time	for RD ↑	T_{RDHD}	C_L = 40pF	-	12	ns
WR signal width		T_{WR}	Note	15	-	ns
Data setup time	for WR ↑	T_{DWR}	-	14	-	ns
Data hold time	for WR ↑	T_{WRD}	-	0	-	ns

Note: When WRQ signal is output, the time will be the interval between WRQ terminal = H level and WR terminal = H level.

8.4.3.2 PCL6125

Item		Name	Condition	Min.	Max.	Unit
Address setup time	for RD ↓	T_{AR}	-	11	-	ns
Address setup time	for WR ↓	T_{AW}	-	0	-	ns
Address hold time	for RD, WR ↑	T_{RWA}	-	0	-	ns
CS setup time	for RD↓	T_{CSR}	-	0	-	ns
CS setup time	for WR ↓	T_{CSW}	-	0	-	ns
CS hold time	for RD, WR ↑	T_{RWCS}	-	0	-	ns
WRQ ON delay time	for CS↓	T_{CSWT}	C_L = 40pF	-	13	ns
WRQ signal L level time		T_{WAIT}	-	-	4･T_{CLK}	ns
Data output delay time	for RD ↓	T_{RDLD}	C_L = 40pF	-	13	ns
Data output delay time	for WRQ ↑	T_{WTHD}	C_L = 40pF	-	8	ns
Data float delay time	for RD ↑	T_{RDHD}	C_L = 40pF	-	12	ns
WR signal width		T_{WR}	Note	15	-	ns
Data setup time	for WR ↑	T_{DWR}	-	15	-	ns
Data hold time	for WR ↑	T_{WRD}	-	0	-	ns

Note: When WRQ signal is output, the time will be the interval between WRQ terminal = H level and WR terminal = H level.

8.4.3.3 PCL6145

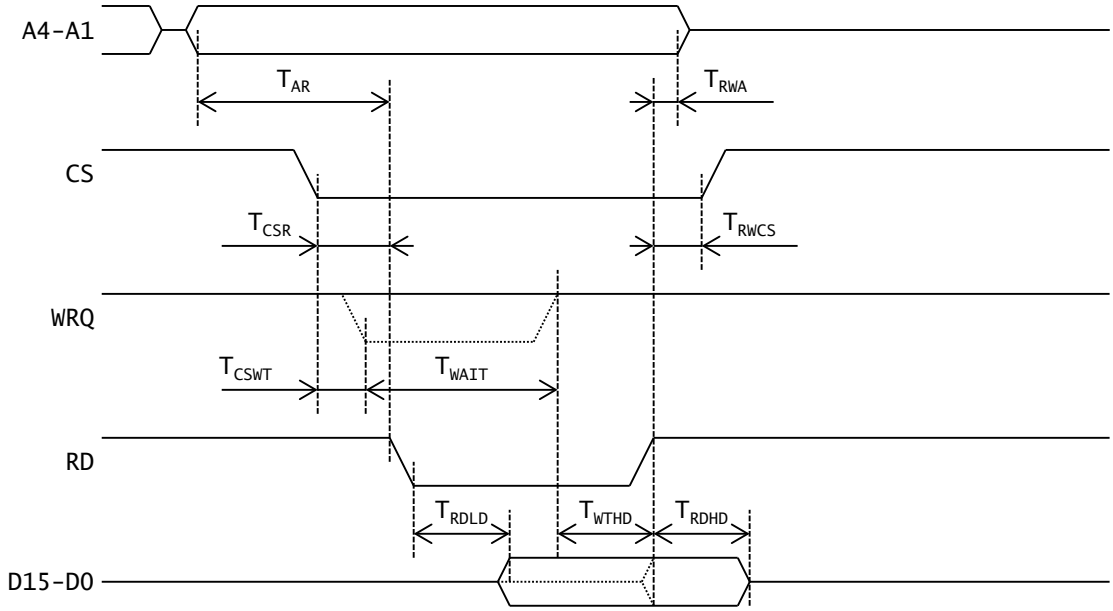
Item		Name	Condition	Min.	Max.	Unit
Address setup time	for RD ↓	T_{AR}	-	12	-	ns
Address setup time	for WR ↓	T_{AW}	-	0	-	ns
Address hold time	for RD, WR ↑	T_{RWA}	-	0	-	ns
CS setup time	for RD↓	T_{CSR}	-	0	-	ns
CS setup time	for WR ↓	T_{CSW}	-	0	-	ns
CS hold time	for RD, WR ↑	T_{RWCS}	-	0	-	ns
WRQ ON delay time	for CS↓	T_{CSWT}	C_L = 40pF	-	13	ns
WRQ signal L level time		T_{WAIT}	-	-	4･T_{CLK}	ns
Data output delay time	for RD ↓	T_{RDLD}	C_L = 40pF	-	14	ns
Data output delay time	for WRQ ↑	T_{WTHD}	C_L = 40pF	-	8	ns
Data float delay time	for RD ↑	T_{RDHD}	C_L = 40pF	-	13	ns
WR signal width		T_{WR}	Note	16	-	ns
Data setup time	for WR ↑	T_{DWR}	-	17	-	ns
Data hold time	for WR ↑	T_{WRD}	-	0	-	ns

Note: When WRQ signal is output, the time will be the interval between WRQ terminal = H level and WR terminal = H level.

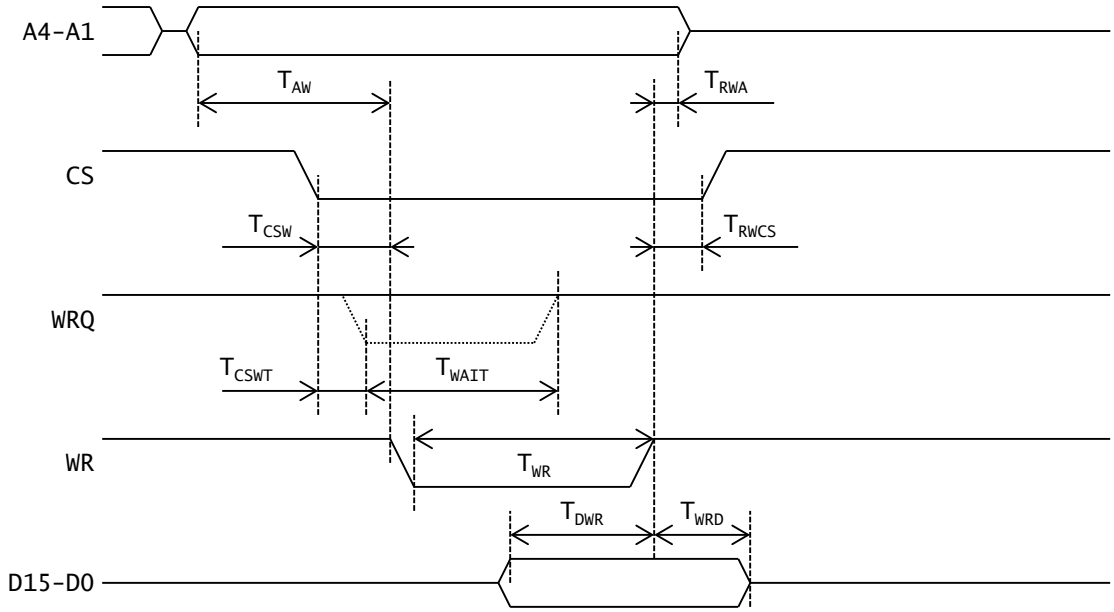
8.4.4 16-bit interface-3 (8086, etc.)

Setting: IF1 terminal = H level, IF0 terminal = L level

<Read cycle>



<Write cycle>



8.4.4.1 PCL6115

Item		Name	Condition	Min.	Max.	Unit
Address setup time	for RD ↓	T_{AR}	-	11	-	ns
Address setup time	for WR ↓	T_{AW}	-	0	-	ns
Address hold time	for RD, WR ↑	T_{RWA}	-	0	-	ns
CS setup time	for RD↓	T_{CSR}	-	0	-	ns
CS setup time	for WR ↓	T_{CSW}	-	0	-	ns
CS hold time	for RD, WR ↑	T_{RWCS}	-	0	-	ns
WRQ ON delay time	for CS ↓	T_{CSWT}	C_L = 40pF	-	13	ns
WRQ signal L level time		T_{WAIT}	-	-	$4 \cdot T_{CLK}$	ns
Data output delay time	for RD ↓	T_{RDLD}	C_L = 40pF	-	13	ns
Data output delay time	for WRQ ↑	T_{WTHD}	C_L = 40pF	-	8	ns
Data float delay time	for RD ↑	T_{RDHD}	C_L = 40pF	-	12	ns
WR signal width		T_{WR}	Note	15	-	ns
Data setup time	for WR ↑	T_{DWR}	-	14	-	ns
Data hold time	for WR ↑	T_{WRD}	-	0	-	ns

Note: When WRQ signal is output, the time will be the interval between WRQ terminal = H level and WR terminal = H level.

8.4.4.2 PCL6125

Item		Name	Condition	Min.	Max.	Unit
Address setup time	for RD ↓	T_{AR}	-	11	-	ns
Address setup time	for WR ↓	T_{AW}	-	0	-	ns
Address hold time	for RD, WR ↑	T_{RWA}	-	0	-	ns
CS setup time	for RD↓	T_{CSR}	-	0	-	ns
CS setup time	for WR ↓	T_{CSW}	-	0	-	ns
CS hold time	for RD, WR ↑	T_{RWCS}	-	0	-	ns
WRQ ON delay time	for CS ↓	T_{CSWT}	C_L = 40pF	-	13	ns
WRQ signal L level time		T_{WAIT}	-	-	$4 \cdot T_{CLK}$	ns
Data output delay time	for RD ↓	T_{RDLD}	C_L = 40pF	-	13	ns
Data output delay time	for WRQ ↑	T_{WTHD}	C_L = 40pF	-	8	ns
Data float delay time	for RD ↑	T_{RDHD}	C_L = 40pF	-	12	ns
WR signal width		T_{WR}	Note	15	-	ns
Data setup time	for WR ↑	T_{DWR}	-	15	-	ns
Data hold time	for WR ↑	T_{WRD}	-	0	-	ns

Note: When WRQ signal is output, the time will be the interval between WRQ terminal = H level and WR terminal = H level.

8.4.4.3 PCL6145

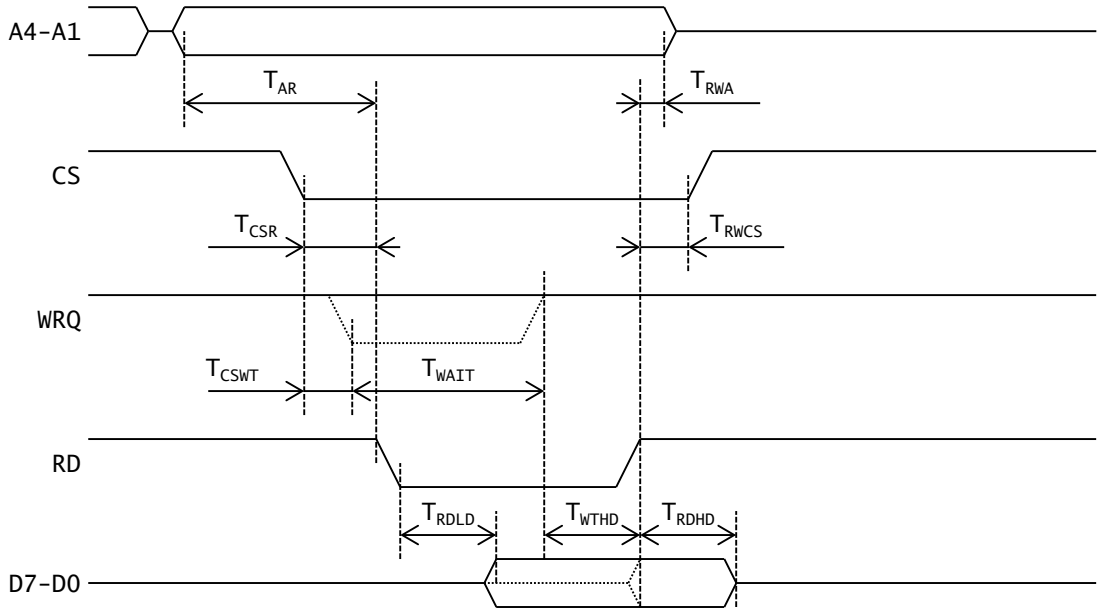
Item		Name	Condition	Min.	Max.	Unit
Address setup time	for RD ↓	T_{AR}	-	12	-	ns
Address setup time	for WR ↓	T_{AW}	-	0	-	ns
Address hold time	for RD, WR ↑	T_{RWA}	-	0	-	ns
CS setup time	for RD↓	T_{CSR}	-	0	-	ns
CS setup time	for WR ↓	T_{CSW}	-	0	-	ns
CS hold time	for RD, WR ↑	T_{RWCS}	-	0	-	ns
WRQ ON delay time	for CS ↓	T_{CSWT}	C_L = 40pF	-	13	ns
WRQ signal L level time		T_{WAIT}	-	-	$4 \cdot T_{CLK}$	ns
Data output delay time	for RD ↓	T_{RDLD}	C_L = 40pF	-	14	ns
Data output delay time	for WRQ ↑	T_{WTHD}	C_L = 40pF	-	8	ns
Data float delay time	for RD ↑	T_{RDHD}	C_L = 40pF	-	13	ns
WR signal width		T_{WR}	Note	16	-	ns
Data setup time	for WR ↑	T_{DWR}	-	17	-	ns
Data hold time	for WR ↑	T_{WRD}	-	0	-	ns

Note: When WRQ signal is output, the time will be the interval between WRQ terminal = H level and WR terminal = H level.

8.4.5 8-bit interface (Z80, etc.)

Setting: IF1 terminal = H level, IF0 terminal = H level

<Read cycle>



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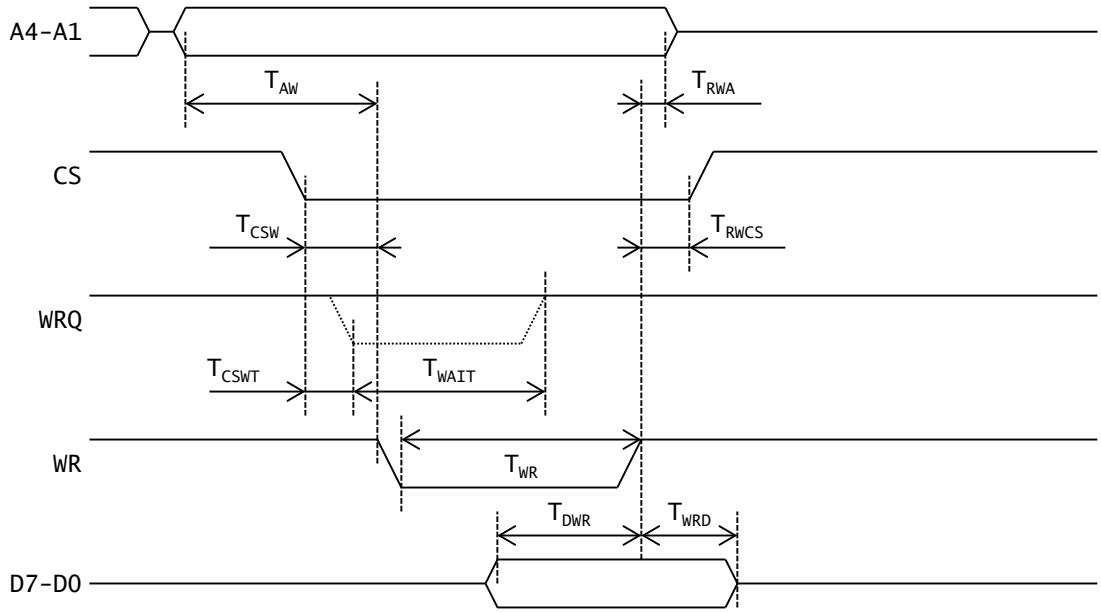


8.4.5.1 PCL6115

Item		Name	Condition	Min.	Max.	Unit
Address setup time	for RD ↓	T_{AR}	-	11	-	ns
Address setup time	for WR ↓	T_{AW}	-	0	-	ns
Address hold time	for RD, WR ↑	T_{RWA}	-	0	-	ns
CS setup time	for RD↓	T_{CSR}	-	0	-	ns
CS setup time	for WR ↓	T_{CSW}	-	0	-	ns
CS hold time	for RD, WR ↑	T_{RWCS}	-	0	-	ns
WRQ ON delay time	for CS ↓	T_{CSWT}	C_L = 40pF	-	13	ns
WRQ signal L level time		T_{WAIT}	-	-	4･T_{CLK}	ns
Data output delay time	for RD ↓	T_{RDLD}	C_L = 40pF	-	13	ns
Data output delay time	for WRQ ↑	T_{WTHD}	C_L = 40pF	-	8	ns
Data float delay time	for RD ↑	T_{RDHD}	C_L = 40pF	-	12	ns
WR signal width		T_{WR}	Note	15	-	ns
Data setup time	for WR ↑	T_{DWR}	-	14	-	ns
Data hold time	for WR ↑	T_{WRD}	-	0	-	ns

Note: When WRQ signal is output, the time will be the interval between WRQ terminal = H level and WR terminal = H level.

8.4.5.2 PCL6125

Item		Name	Condition	Min.	Max.	Unit
Address setup time	for RD ↓	T_{AR}	-	11	-	ns
Address setup time	for WR ↓	T_{AW}	-	0	-	ns
Address hold time	for RD, WR ↑	T_{RWA}	-	0	-	ns
CS setup time	for RD↓	T_{CSR}	-	0	-	ns
CS setup time	for WR ↓	T_{CSW}	-	0	-	ns
CS hold time	for RD, WR ↑	T_{RWCS}	-	0	-	ns
WRQ ON delay time	for CS ↓	T_{CSWT}	C_L = 40pF	-	13	ns
WRQ signal L level time		T_{WAIT}	-	-	4･T_{CLK}	ns
Data output delay time	for RD ↓	T_{RDLD}	C_L = 40pF	-	13	ns
Data output delay time	for WRQ ↑	T_{WTHD}	C_L = 40pF	-	8	ns
Data float delay time	for RD ↑	T_{RDHD}	C_L = 40pF	-	12	ns
WR signal width		T_{WR}	Note	15	-	ns
Data setup time	for WR ↑	T_{DWR}	-	15	-	ns
Data hold time	for WR ↑	T_{WRD}	-	0	-	ns

Note: When WRQ signal is output, the time will be the interval between WRQ terminal = H level and WR terminal = H level.

8.4.5.3 PCL6145

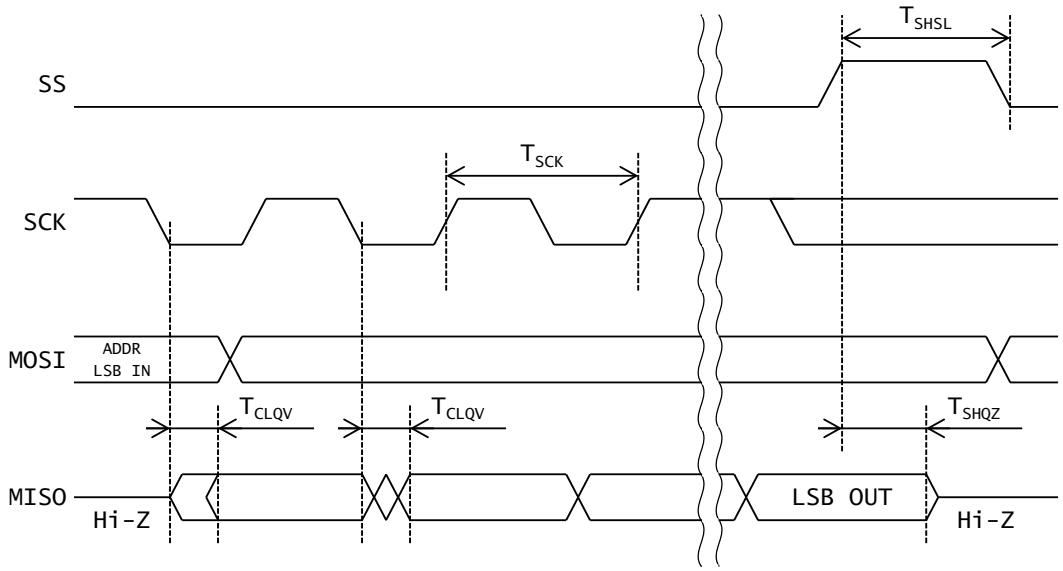
Item		Name	Condition	Min.	Max.	Unit
Address setup time	for RD ↓	T_{AR}	-	12	-	ns
Address setup time	for WR ↓	T_{AW}	-	0	-	ns
Address hold time	for RD, WR ↑	T_{RWA}	-	0	-	ns
CS setup time	for RD ↓	T_{CSR}	-	0	-	ns
CS setup time	for WR ↓	T_{CSW}	-	0	-	ns
CS hold time	for RD, WR ↑	T_{RWCS}	-	0	-	ns
WRQ ON delay time	for CS ↓	T_{CSWT}	C_L = 40pF	-	14	ns
WRQ signal L level time		T_{WAIT}	-	-	4･T_{CLK}	ns
Data output delay time	for RD ↓	T_{RDLD}	C_L = 40pF	-	14	ns
Data output delay time	for WRQ ↑	T_{WTHD}	C_L = 40pF	-	8	ns
Data float delay time	for RD ↑	T_{RDHD}	C_L = 40pF	-	13	ns
WR signal width		T_{WR}	Note	16	-	ns
Data setup time	for WR ↑	T_{DWR}	-	17	-	ns
Data hold time	for WR ↑	T_{WRD}	-	0	-	ns

Note: When WRQ signal is output, the time will be the interval between WRQ terminal = H level and WR terminal = H level.

8.4.6 Serial interface

Setting: RD = L level, WR = L level

<Read cycle>



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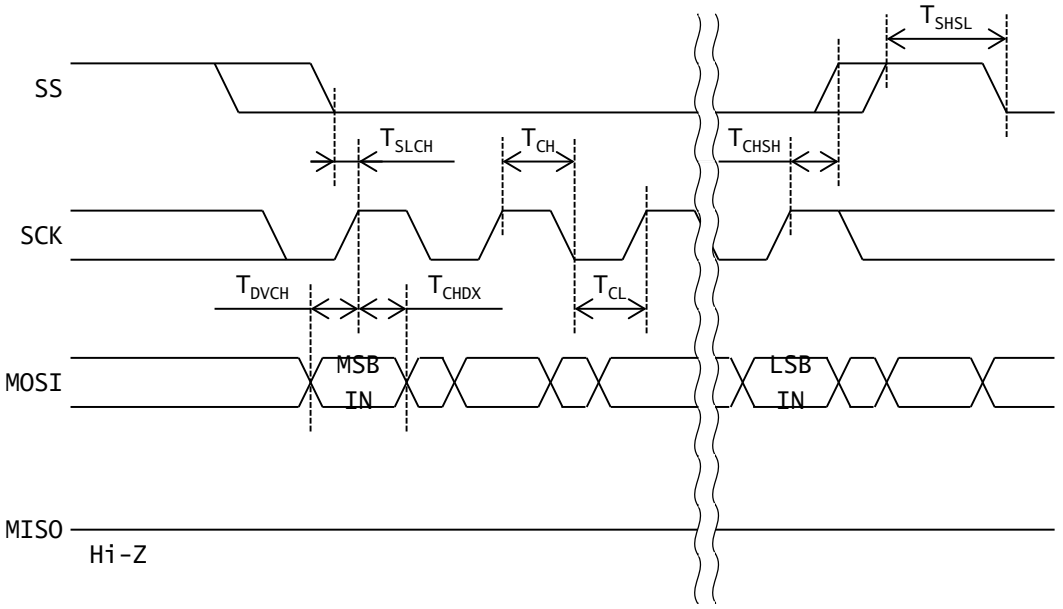


8.4.6.1 PCL6115

Item	Name	Condition	Min	Max	Unit
Serial clock frequency	f_{SCK}	-	-	$f_{CLK}/1.5$	MHz
Serial clock cycle	T_{SCK}	-	-	50	ns
Serial clock H time	T_{CH}	-	20	-	ns
Serial clock L time	T_{CL}	-	20	-	ns
SS signal active setup	T_{SLCH}	-	$10+T_{CLK}$	-	ns
SS signal deselect time	T_{SHSL}	-	$4 \cdot T_{CLK}$	-	ns
SS signal active hold time	T_{CHSH}	-	0	-	ns
Data setup time	T_{DVCH}	-	3	-	ns
Data hold time	T_{CHDX}	-	1	-	ns
Output disable time	T_{SHQZ}	C_L=40pF	-	$16+T_{CLK}$	ns
Output delay time	T_{CLQV}	C_L=40pF	-	20	ns

8.4.6.2 PCL6125

Item	Name	Condition	Min	Max	Unit
Serial clock frequency	f_{SCK}	-	-	$f_{CLK}/1.5$	MHz
Serial clock cycle	T_{SCK}	-	-	50	ns
Serial clock H time	T_{CH}	-	20	-	ns
Serial clock L time	T_{CL}	-	20	-	ns
SS signal active setup	T_{SLCH}	-	$10+T_{CLK}$	-	ns
SS signal deselect time	T_{SHSL}	-	$4 \cdot T_{CLK}$	-	ns
SS signal active hold time	T_{CHSH}	-	0	-	ns
Data setup time	T_{DVCH}	-	2	-	ns
Data hold time	T_{CHDX}	-	1	-	ns
Output disable time	T_{SHQZ}	C_L=40pF	-	$18+T_{CLK}$	ns
Output delay time	T_{CLQV}	C_L=40pF	-	19	ns

8.4.6.3 PCL6145

Item	Name	Condition	Min	Max	Unit
Serial clock frequency	f_{SCK}	-	-	$f_{CLK}/1.5$	MHz
Serial clock cycle	T_{SCK}	-	-	50	ns
Serial clock H time	T_{CH}	-	20	-	ns
Serial clock L time	T_{CL}	-	20	-	ns
SS signal active setup	T_{SLCH}	-	$10+T_{CLK}$	-	ns
SS signal deselect time	T_{SHSL}	-	$4 \cdot T_{CLK}$	-	ns
SS signal active hold time	T_{CHSH}	-	0	-	ns
Data setup time	T_{DVCH}	-	3	-	ns
Data hold time	T_{CHDX}	-	1	-	ns
Output disable time	T_{SHQZ}	C_L=40pF	-	$20+T_{CLK}$	ns
Output delay time	T_{CLQV}	C_L=40pF	-	19	ns

8.5 Operation timing (common for all axes)

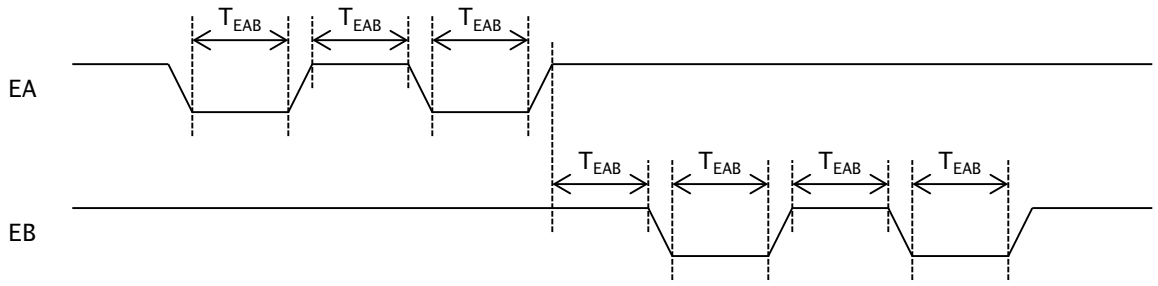
Input signal width is a pulse width that can be recognized; output signal width is a pulse width to be output.

Min/Max is the time required to be processed.

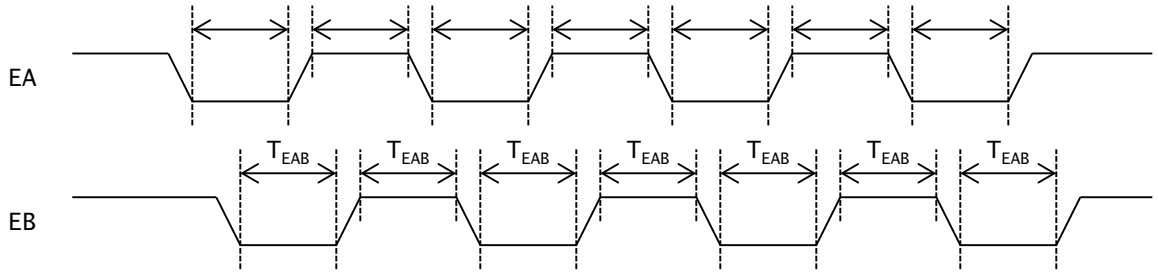
Item		Name	Condition	Min.	Max.	Unit
RST input signal width		-	Note	8・T_{CLK}	-	ns
EAn, EBn, EZn input signal width		T_{EAB}	RENV2.EINF = 0	2・T_{CLK}	-	ns
			RENV2.EINF = 1	3・T_{CLK}	-	
PAn, PBn input signal width		T_{PAB}	RENV2.PINF = 0	2・T_{CLK}	-	ns
			RENV2.PINF = 1	3・T_{CLK}	-	
ERCn output signal width		-	RENV1.EPW = 000b	225・T_{CLK}	240・T_{CLK}	ns
			RENV1.EPW = 001b	1793・T_{CLK}	1920・T_{CLK}	
			RENV1.EPW = 010b	7169・T_{CLK}	7680・T_{CLK}	
			RENV1.EPW = 011b	28673・T_{CLK}	30720・T_{CLK}	
			RENV1.EPW = 100b	229377・T_{CLK}	245760・T_{CLK}	
			RENV1.EPW = 101b	917505・T_{CLK}	983040・T_{CLK}	
			RENV1.EPW = 110b	1835009・T_{CLK}	1966080・T_{CLK}	
			RENV1.EPW = 111b	(Level output)		
Off timer time of deviation counter clear signal		-	RENV1.ETW = 01b	225・T_{CLK}	240・T_{CLK}	ns
			RENV1.ETW = 10b	28673・T_{CLK}	30720・T_{CLK}	
			RENV1.ETW = 11b	1835009・T_{CLK}	1966080・T_{CLK}	
PELn, MELn, SDn, ORGn, ALMn, INPn, CEMG input signal width		-	RENV1.FLTR = 0	2・T_{CLK}	-	ns
			RENV1.FLTR = 1 & RENV1.FTM = 00b	64・T_{CLK}	-	
			RENV1.FLTR = 1 & RENV1.FTM = 01b	512・T_{CLK}	-	
			RENV1.FLTR = 1 & RENV1.FTM = 10b	4096・T_{CLK}	-	
			RENV1.FLTR = 1 & RENV1.FTM = 11b	32768・T_{CLK}	-	
PDRn, MDRn, PEn input signal width		-	RENV1.DRF = 0	2・T_{CLK}	-	ns
			RENV1.DRF = 1	1048576・T_{CLK}	-	
Time of direction change timer		-	RENV1.DTMF = 0	3585・T_{CLK}	3840・T_{CLK}	ns
			RENV1.DTMF = 1	10・T_{CLK}		
PCSn input signal width		-	-	2・T_{CLK}	-	ns
LTCn input signal width		-	-	2・T_{CLK}	-	ns
CSTA	Output signal width	-	-	8・T_{CLK}		ns
	Input signal width	-	-	4・T_{CLK}	-	ns
CSTP	Output signal width	-	-	8・T_{CLK}		ns
	Input signal width	-	-	4・T_{CLK}	-	ns
BSYn signal ON delay time		T_{CMDBSY}	-	4・T_{CLK}	5・T_{CLK}	ns
		T_{STABSY}	-	4・T_{CLK}	5・T_{CLK}	ns
Start delay time		T_{CMDPLS}	-	15・T_{CLK}	16・T_{CLK}	ns
		T_{STAPLS}	-	15・T_{CLK}	16・T_{CLK}	ns
Deceleration delay time		T_{CMDFDW}	-	5・T_{CLK}	6・T_{CLK}	ns
		T_{SDFDW}	-	2・T_{CLK}	3・T_{CLK}	ns

Note: It is necessary to input eight or more CLK signals while "RST = L level".

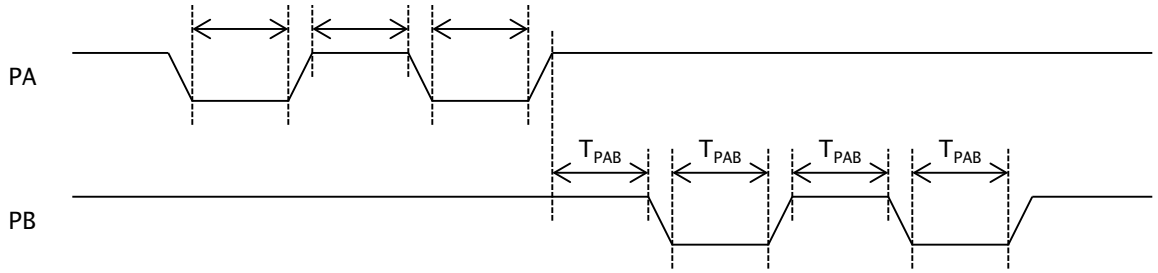
8.5.1 Encoder signal input (2-pulse mode)



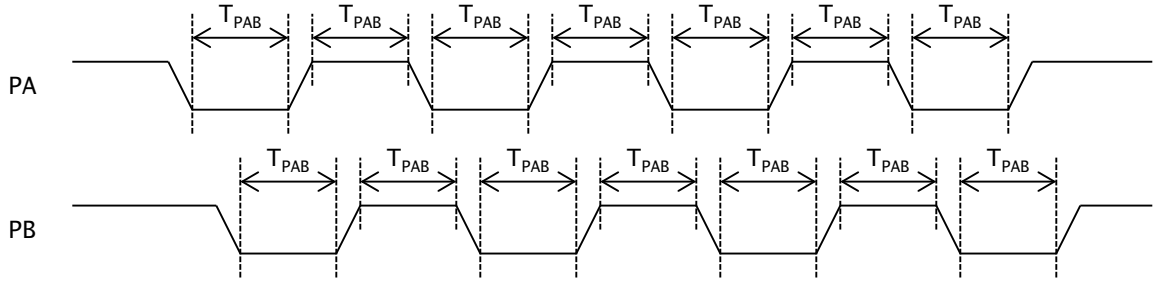
8.5.2 Encoder signal input (90-degree phase difference mode)



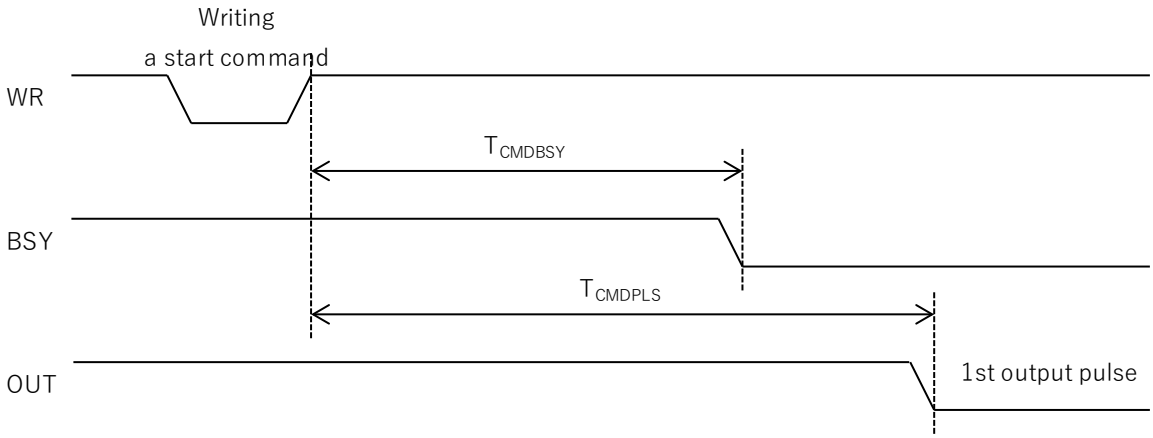
8.5.3 Manual pulser signal input (2-pulse mode)



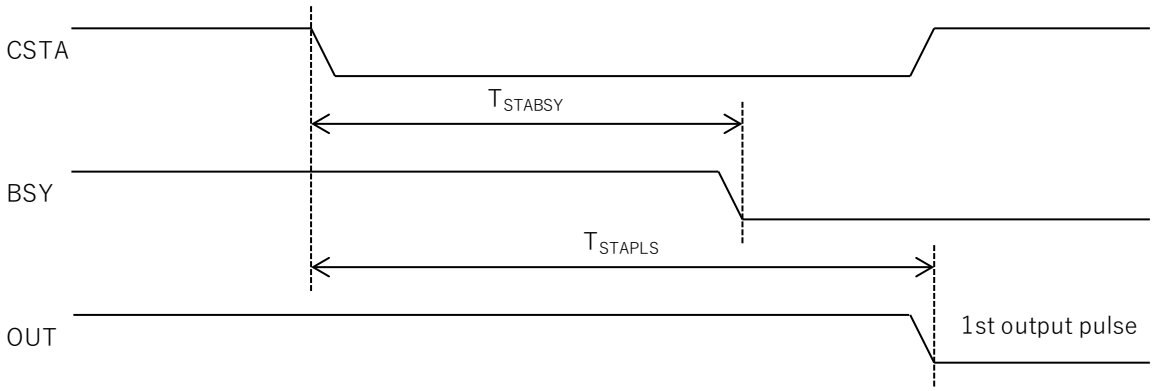
8.5.4 Manual pulser signal input (90-degree phase difference mode)



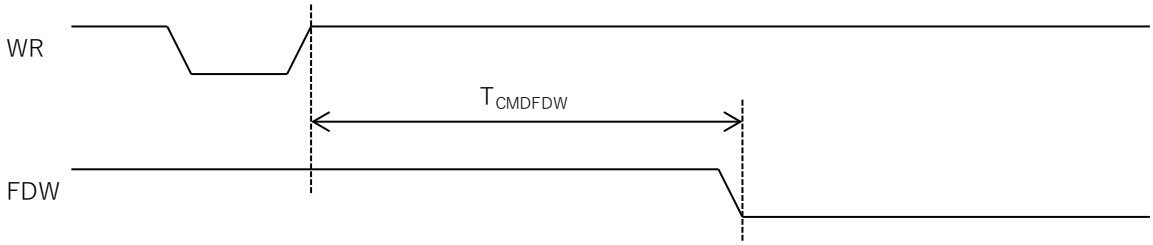
8.5.5 To start an operation by writing a start command:



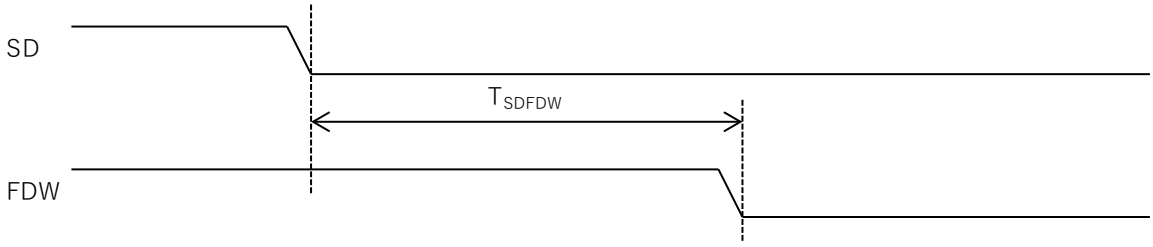
8.5.6 To start an operation by simultaneous start signal input:



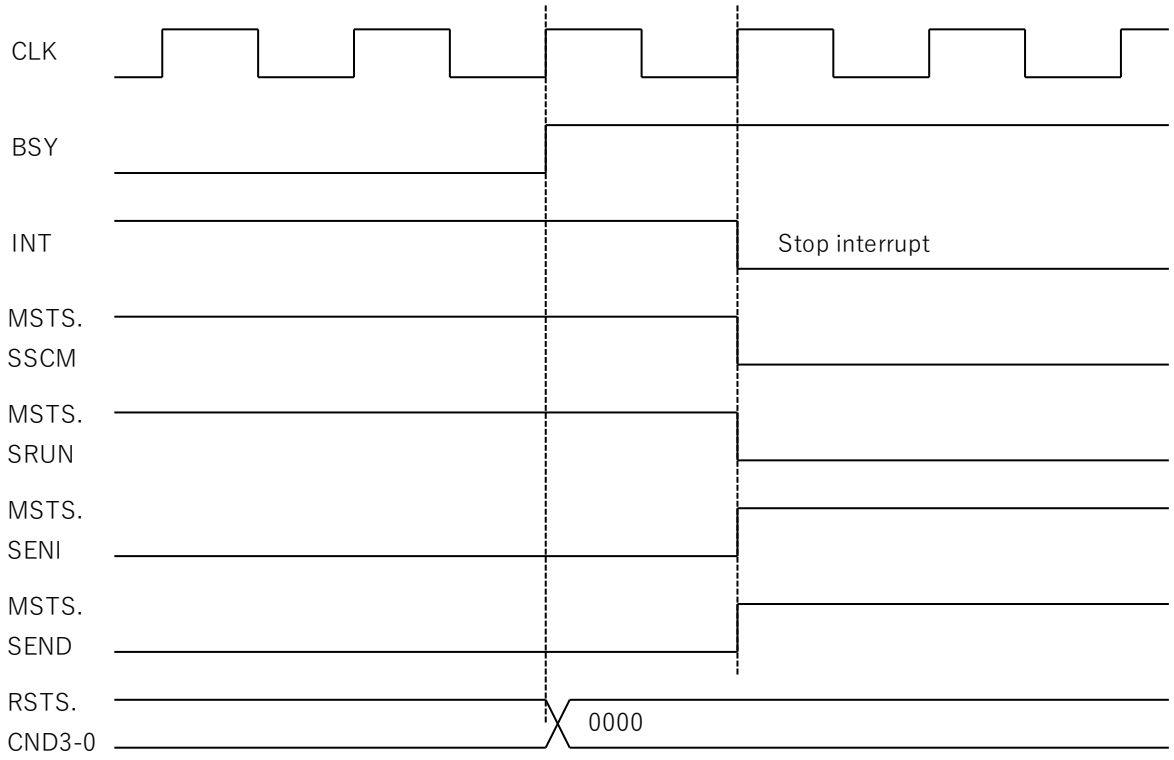
8.5.7 To start decelerating by slow-down FL speed change or writing deceleration stop command:



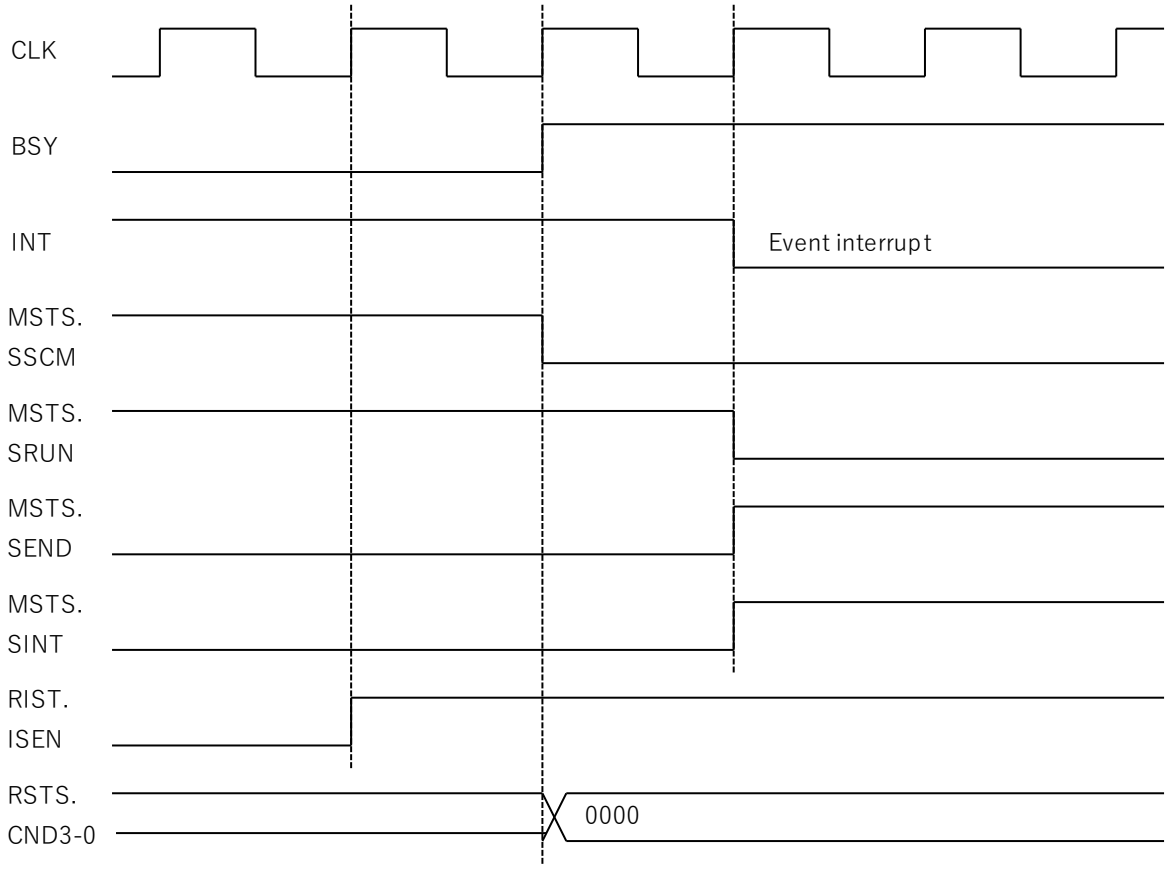
8.5.8 To start decelerating by slow-down signal input:



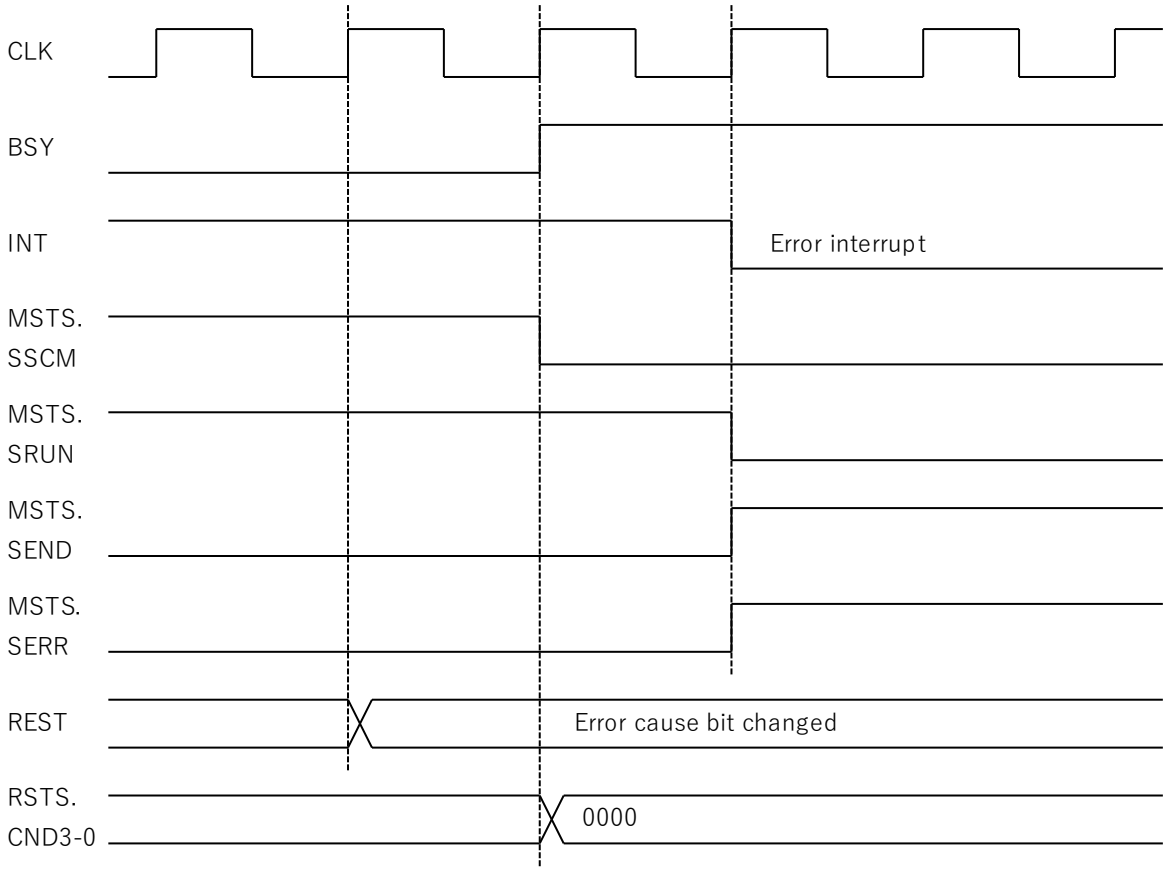
8.5.9 Immediate stop command writing (continuous movement operation mode):



8.5.10 Normal stop (incremental movement operation mode):



8.5.11 Abnormal stop (incremental movement operation mode):



9. Handling Precautions

9.1 Design precautions

1. Regarding operating voltage, current, temperature, I/O voltage / current etc., please use this product within the rated range. If used outside the rating range, even if it operates normally in the short term, there is a possibility of increasing the failure rate.
   Even within the rated range, the failure rate varies depending on the operating temperature and voltage, so please consider this point when designing the equipment.
   Furthermore, please do not exceed absolute maximum ratings even for a very short time.
2. Take precautions against the influence of heat in the environment and keep the temperature around the LSI as cool as possible.
3. Please note that ignoring the following may result in latching up and may cause overheating and smoke.
   - Make sure that the voltage on the I/O terminals does not exceed the maximum ratings.
   - Consider power voltage drop timing when turning ON/OFF the power.
   - Be careful not to introduce external noise into the LSI.
   - Fix the unused input terminals to +3.3 V or GND level or need to be pulled-up or pulled down.
   - Do not short-circuit the outputs.
   - Protect the LSI from inductive pulses caused by electrical sources that generate large voltage surges and take appropriate precautions against static electricity.
4. Provides external circuit protection components so that overvoltage caused by noise, voltage surges, or static electricity is not fed to the LSI.

9.2 Precautions for transporting and storing LSIs

1. Always handle LSIs and their packages carefully. Throwing or dropping LSIs may damage them or may cause damage to airtightness by breaking packaging of aluminum laminate
2. Do not store LSIs in a location exposed to water droplets or direct sunlight.
3. Do not store the LSI in a location where corrosive gases are present, or in excessively dusty environments.
4. Store the LSIs in an anti-static storage container, and make sure that no physical load is placed on the LSIs.
5. When transporting, follow the cautions on the packaging box.
6. The storage temperature should be 5 to 35 °C and humidity should be 40 to 70% as a guide.
7. Keep LSIs in a place with little temperature change. Drastic temperature change during storage leads to condensation, lead wire oxidation, corrosion, etc., and causes bad solder wettability.
8. Place an antistatic mat on the storage shelf surface and ground the mat's surface. (Surface-earth resistance between 7.5×10^5 and 1×10^9 Ω)
9. When removing the LSI from packaging and storing it again, please use the antistatic storage container.

9.3 Precautions for handling environment

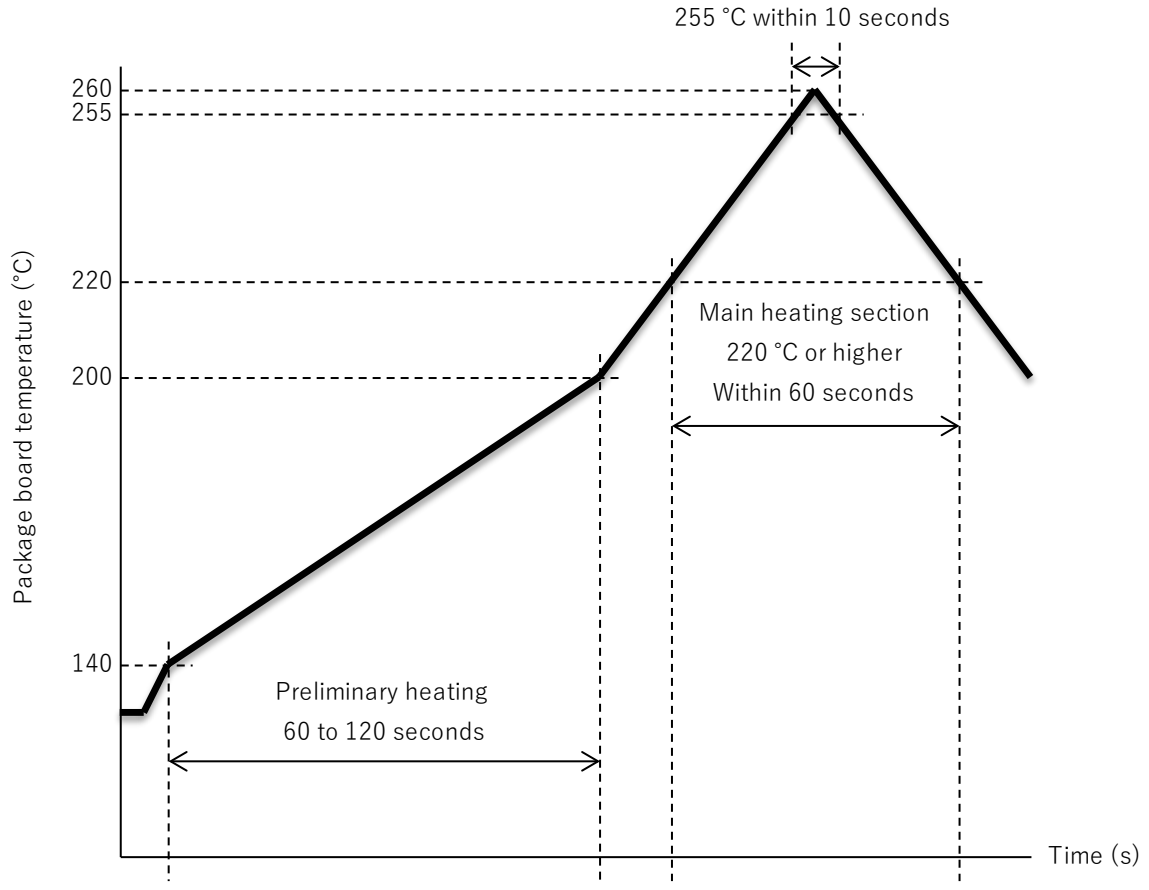
1. The humidity should be 40 to 60% considering moisture absorption after opening moisture-proof packaging products.
2. Make sure to ground all equipment, tools, and jigs that are present at the work site.
3. Ground the work floor using a conductive mat or similar apparatus (with an appropriate resistance factor) (Surface-earth resistance should be 1×10^9 Ω or less)
4. Ground the work desk surface using a conductive mat (Surface-earth resistance should be 7.5×10^5 to 10^9 Ω).
5. Do not allow work on a metal surface, which can cause a rapid change in the electrical charge on the LSI (if the charged LSI touches the surface directly) due to extremely low resistance.
6. When picking up an LSI using a vacuum device, provide anti-static protection using a conductive rubber pick up tip.
7. Do not touch LSI with electrified body (such as working wear, human body, etc.).
8. The surface of the display (such as cathode ray tube etc.) in the work area should be shielded from static electricity by OA equipment filter etc. Avoid turning ON / OFF during operation as much as possible.
9. Please use a conductive cover, conductive caster, etc. on the work chair and ground it to the floor. (Seat surface - ground resistance should be 1×10^{10} Ω or less)
10. Workers should wear a wrist strap and ground with resistance.
    (When worn, the resistance between the surface and earth should be 7.5×10^5 to 3.5×10^7 Ω).
11. Handle the LSI package and the LSI carefully so as not to subject them to mechanical vibrations and impact.

9.4 Precautions for installation

1. Plastic packages absorb moisture easily. Even if they are stored indoors, they will absorb moisture as time passes. If LSI that has absorbed moisture is put into a solder reflow furnace, cracks may occur in the resin or adhesion between the resin and the frame may deteriorate. Storage period before moisture proof bag opening is one year.

2. If you are worried about moisture absorption, dry the packages thoroughly before reflowing the solder.
   Dry the packages for 20 hours or more to 36 hours or less at 125 ± 5 °C. They can be dried up to two times.
   If seven days passes after opening moisture proof bag, the LSI will need to be dried.

3. If you will be using a soldering method that heats the whole package and you are worried about moisture absorption, dry the packages thoroughly before reflowing the solder.
   - The temperature profile of an infrared reflow furnace must be within the range shown in the figure below. (The temperatures shown are for the temperature at the surface of the plastic package.)
   - The chlorine content (mass percentage) of rosin flux is recommended to be 0.2% or less.



[Profile (Lead-free solder mounting compatible)]

4. Solder dipping causes rapid temperature changes in the packages and may damage the devices. Therefore, do not use this method.
5. Hand soldering work using a solder iron should be done under the following conditions.
   - Maximum temperature of the soldering iron 350 °C, max. 5 seconds or less (per terminal).
   - Be careful that the solder iron does not touch parts other than the lead part, such as the package body.

Revision

Revision	Date	Contents
First	May 9, 2018	New document
Second	April 5, 2019	Overall layouts and contents are revised from the first version.

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