Pulse Control LSI

With Sequencing Function for Stepper Motors

PCD4600 Series

PCD4611A
PCD4621A
PCD4641A

User's Manual

(Replacement version

from PCD4500/PCD45x1 series)

Nippon Pulse Motor Co., Ltd.

■ Preface and cautions

[Preface]

Thank you for considering our pulse control LSI, the "PCD46x1A series."
Before using the product, read this manual to become familiar with the product.
Please note that the section "Handling precautions" which includes details about mounting this LSI can be found at the end of this manual.

[Cautions]

(1) Copying all or any part of this manual without written approval is prohibited.
(2) The specifications of this LSI may be changed to improve performance or quality without prior notice.
(3) Although this manual was produced with the utmost care, if you find any points that are unclear, wrong, or have inadequate descriptions, please let us know.
(4) We are not responsible for any results that occur from using this LSI, regardless of item (3) above.
(5) If you use it in any device that may require high quality and reliability, or where faults or malfunctions may directly affect human survival or injure humans, such as in nuclear power control devices, aviation devices or spacecraft, traffic signals, fire control, or various types of safety devices, we will not be liable for any problem that occurs, even if it was directly caused by the LSI. Customers must provide their own safety measures to ensure appropriate performance in all circumstances.

■ Replacement version from PCD4500 / PCD45x1 series

This document is for replacement version of PCD4500 / PCD4511 / PCD4521 / PCD4541.
The PCD 46x1A series' software is downward compatible with the PCD4500 / PCD4511 / PCD4521 / PCD4541. When you use it within the conventional models' functions, you can use the conventional software with confirming added bits. When using previously existing software designed for the PCL4500/PCD4511/PCD4521/ PCD4541, please see “8-2. Compatible mode setting”.
The PCD46x1A series chips have some functions added to the conventional models. This document mainly shows description in the case that you use these new functions as the PCD46x1 mode.

Regarding, hardware compatibility, attencion is required. Please see “14-1-7. Precautions in the case of use with parallel I/F”.

■ Descriptions of indicators that are used in this manual

1. PCD46x1A shows PCD4611A, PCD4621A and PCD4641A.
2. The "x" "y" "z" and "u" with terminal names refer to X axis, Y axis, Z axis and U axis, respectively. PCD4611A's terminal names do not have axis name. Comparing with PCD4621A or PCD4641A, please regard an axis name as X axis.
3. The signals such as SD, EL, or PO that have + and – mean both signals unless + or – is shown.
4. Terminals' logic shows in Table 3-1 PCD46x1A Terminal Function List Table
5. A specified bit of registers or commands is referred to as (register / command name).(bit name) (ex. RMD.MSDE). If a bit has a unique meaning, register or command name may be omitted.
6. When describing bits in registers, "n" refers to a bit position. "0" refers to a bit position and means that it is prohibited to write any other than "0" and this bit will always show "0" when it is read.
7. Unless otherwise described, time description affected by the reference clock frequency discussed in this manual is in the case of reference clock 4.9152 [MHz].
8. "b" with numerical number means binary, "h" with numerical number is hexadecimal and only numerical number means decimal.
9. Positive sign of current value of electrical specifications means current value to flow into and negative sign means one to flow out.

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1. Outline and features

1-1. Outline

PCD46x1A is a pulse control LSI with phase sequence control for 2-phase stepper motors. Using these LSIs and ICs for stepping motor drive allows you to construct a stepper motor control system. Inputting data and commands from CPU allows you to control speed and positioning, etc.

1-2. Features

- 3.3 V single power source (Input, output and input / output terminals have 5 V tolerance feature.)
- Maximum output frequency
  4.91 [Mpps] (Reference clock : 9.8304 [MHz], speed magnification : 300x)
  2.46 [Mpps] (Reference clock : 4.9152 [MHz], speed magnification : 300x)
- Two CPU I/F modes are available: parallel (8 bit) and serial (synchronous 4-wire serial).
- Excitation sequencing output for 2-phase stepper motor.
  Unipolar / bipolar
  2-2 phase excitation / 1-2 phase excitation
- Four terminals for excitation sequence output can be used as general-purpose I/O terminals.
- Pulse train output (CW and CCW pulses, pulse and direction signals.)
- Linear and S-curve acceleration / deceleration control.
- External start / stop control
- Continuous operation / origin return operation/ positioning operation / timer operation
- Idling pulse output
- Current position counter (24 bit)
- Automatic setting for a ramping-down point.
- Selection of stop method by ORG, +EL, -EL and STP signals. (Immediate stop / deceleration stop)
- 3 models for single axis (PCD4611A), 2- axis (PCD4621A), and 4- axis (PCD4641A) are available.

2. Specifications

Table 2-1 PCD46x1A main specifications

Item	Standard
Power source	3.0 ~ 3.6[V]
Reference clock	4.9152 [MHz] standard (Max. 10 [MHz])
CPU I/F	Parallel I/F: 8-bit Serial I/F: Synchronous 4-wire serial Serial clock: up to twice of reference clock(upper limit 15[MHz])
Number of control axes	PCD4611A: 1 axis PCD4621A: 2 axes PCD4641A: 4 axes
Positioning pulses setting range	0 ~ 16,777,215 pulses (24-bit)
Speed setting step range	1 ~ 8,191 steps (13-bit)
Recommended speed magnification range	1x ~ 300 x (when using reference clock :4.9152 [MHz]) When 1 x, 1 ~ 8,191 [pps] When 2 x, 2 ~ 16,382 [pps] When 5 x, 5 ~ 40,955 [pps] When 10 x, 10 ~ 81,910 [pps] When 20 x, 20 ~ 163,820 [pps] When 50 x, 50 ~ 409,550 [pps] When 100 x, 100 ~ 819,100 [pps] When 200 x, 200 ~ 1,638,200 [pps] When 300 x, 300 ~ 2,457,300 [pps]
Number of registers for setting the speed	Two per axis for FL and FH speed
Ramping-down point setting range	0 ~ 16,777,215 (24 bit per axis)
Ramping-down point setting method	Manual setting or automatic setting
Acceleration / deceleration method	Linear and S-curve acceleration / deceleration
Acceleration / deceleration rate setting range	1 ~ 65,535 (16 bits per axis)
Current position counters	24-bit up / down counters one circuit / axis
Mechanical sensor input	The following five signals are input per axis ORG (Origin position) +EL, -EL (End limit) +SD, -SD (Ramping-down)
Typical operations	- Continuous operation - Origin return operation - Positioning operation - Timer operation

Item	Standard
Typical functions	- Linear acceleration and deceleration / S-curve acceleration and deceleration - Immediate stop and decelerating stop - Speed change - External start and external stop function - Idling pulse output function - Excitation sequencing output for 2-phase stepper motor - 4 general-purpose input and output ports / axis (They also can be used as sequence output) - 6 common ports (available only with serial I/F)
Ambient operating temperature	-40 ~ +85 [°C]
Storage temperature	-65 ~ +150 [°C]
Package	PCD4611A: 48-pin QFP (Mold section: 7.0 [mm] × 7.0 [mm]) PCD4621A: 64-pin QFP (Mold section: 10.0 [mm] × 10.0 [mm]) PCD4641A:100-pin QFP (Mold section: 14.0 [mm] × 14.0 [mm])
Chip design	C-MOS

3. Terminal

3-1. Terminal assignment diagrams

3-1-1. Terminal assignment diagram of PCD4611A

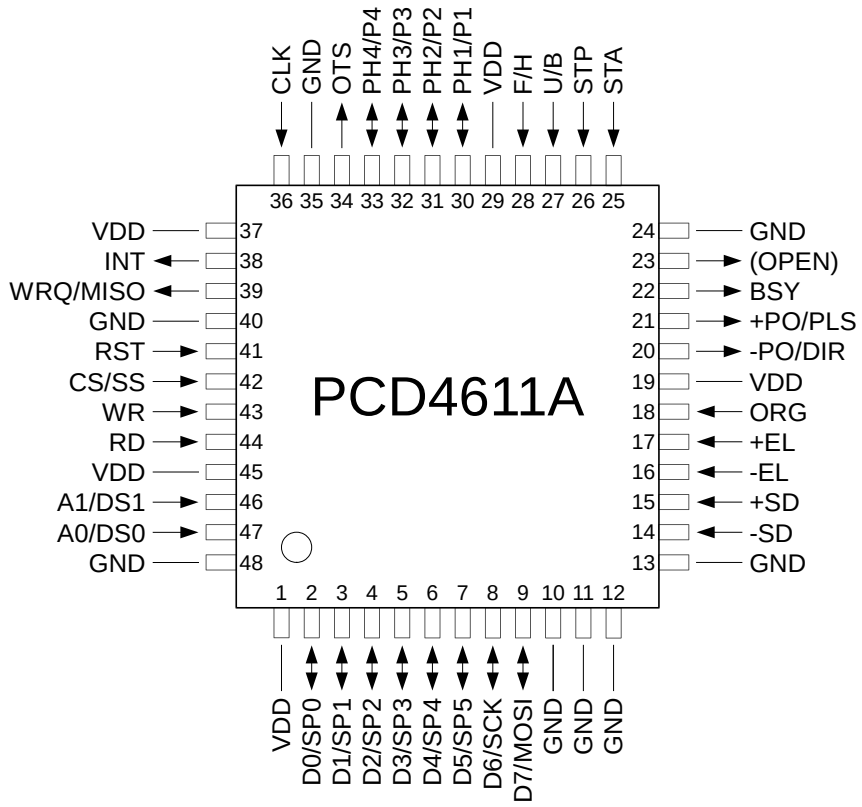


Figure 3-1 Terminal assignment diagram of PCD4611A (Top View)

3-1-2. Terminal assignment diagram of PCD4621A

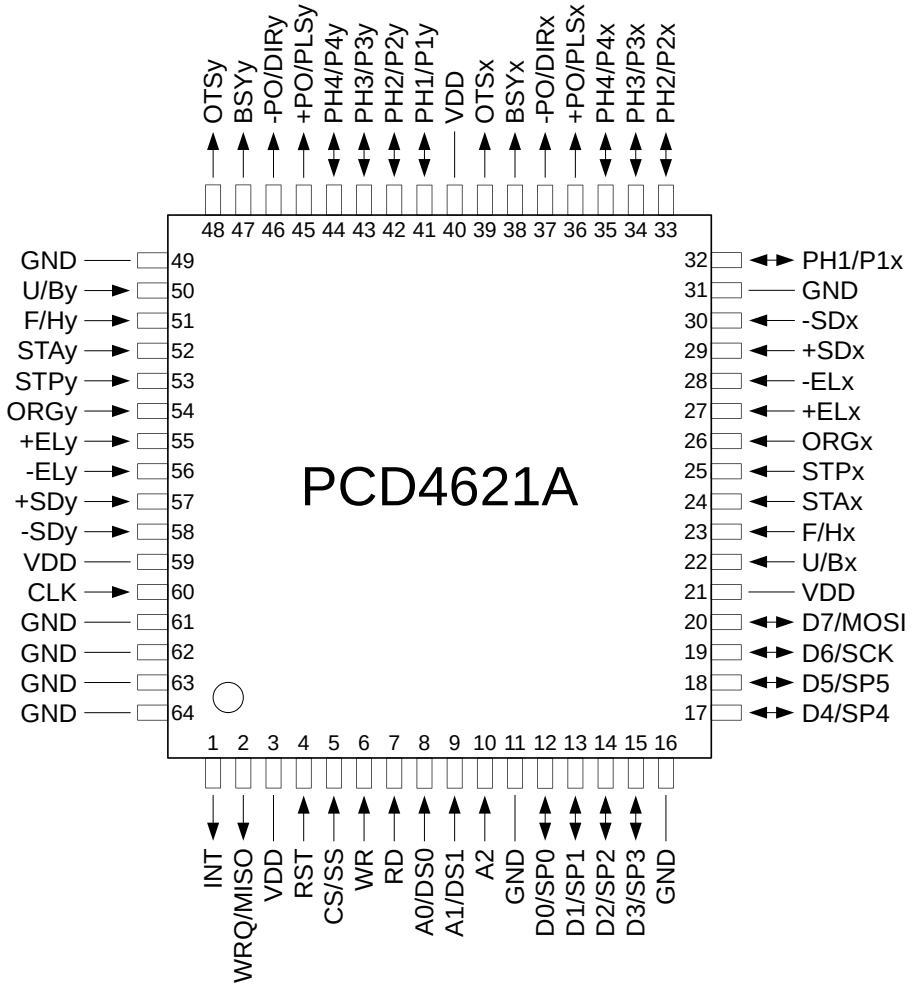


Figure 3-2 Terminal assignment diagram of PCD4621A (Top View)

3-1-3. Terminal assignment diagram of PCD4641A

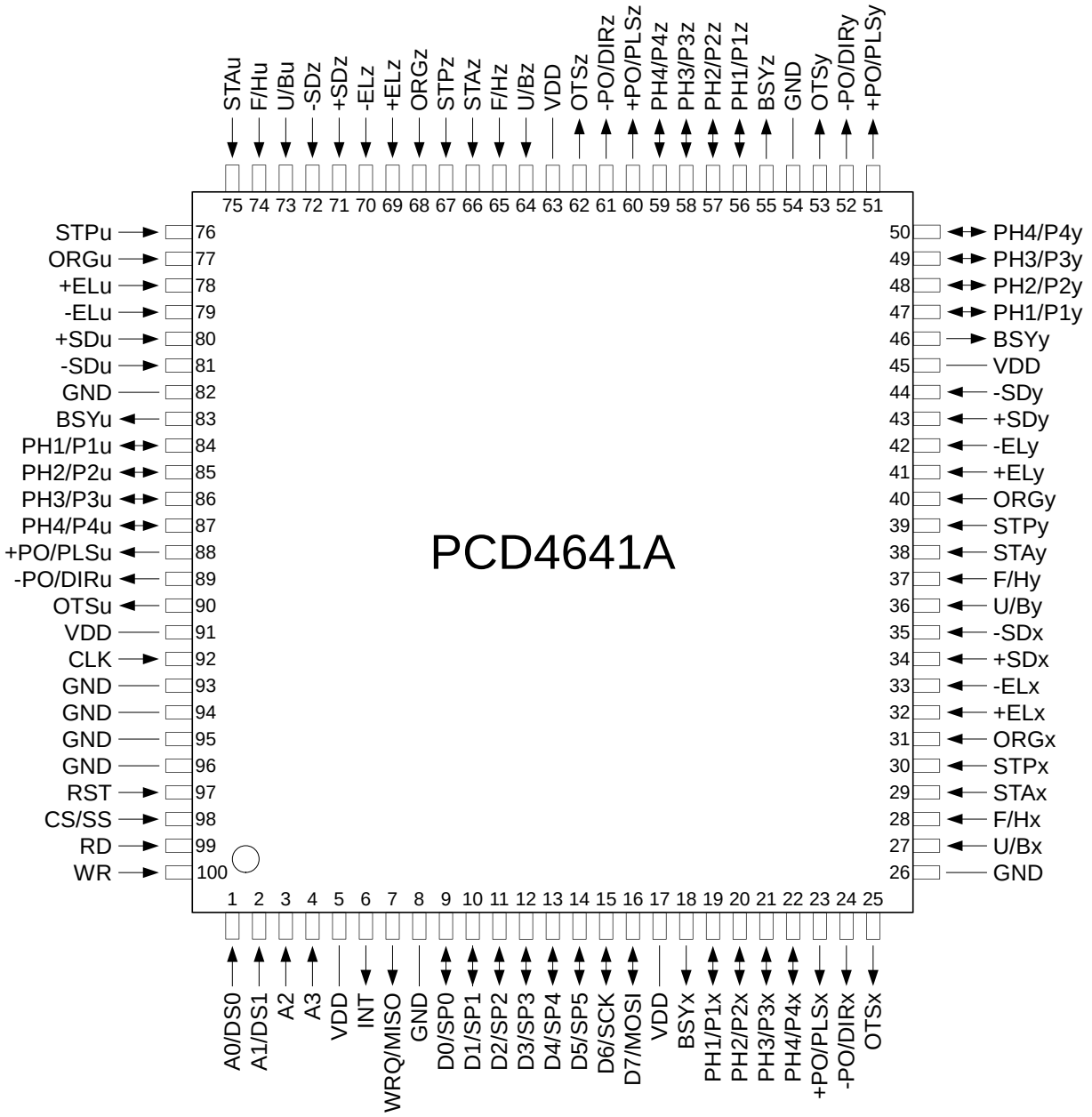


Figure 3-3 Terminal assignment diagram of PCD4641A (Top View)

3-2. Terminal function list

Table 3-1 PCD46x1A Terminal Function List Table

Terminal name	Terminal No. PCD 4611A	PCD 4621A	PCD 4641A	I/O	Logic	Description	5V tolerant
CLK	36	60	92	I	-	Reference clock signal In standard, it inputs clock from oscillator of 4.9152[MHz] (3.3[V] power source).	O
RST	41	4	97	I %	Nega -tive	Reset signal. Reset by inputting L level signal input of 3 cycle reference clock. See“11-1. Reset” in detail.	O
CS/SS	42	5	98	I	Nega -tive	CPU I/F signal With parallel I/F: Chip selection signal (CS) In the case of L level, RD terminal and WR terminal are enabled. With serial I/F: Slave selection signal (SS). See “5. CPU I/F” in detail.	O
WR RD	43 44	6 7	100 99	I	Nega -tive	CPU I/F signal CPU I/F is set by input status at reset. See “5-1-1-2 Selection of CPU I/F” in detail. With parallel I/F: WR: write signal RD: read signal Note: These terminals should be pulled up externally with parallel I/F. With serial I/F: Unused (fixed to L level) See “5. CPU I/F” in detail.	O
A0/DS0 A1/DS1 A2 A3	47 46 - -	8 9 10 -	1 2 3 4	I	Posi -tive	CPU I/F signal With parallel I/F: Address bus (A0 ~ A3) With serial I/F: Device selection No. (only DS0 and DS1 are used.) See “5. CPU I/F” in detail.	O
D0/SP0 D1/SP1 D2/SP2 D3/SP3 D4/SP4 D5/SP5 D6/SCK D7/MOSI	2 3 4 5 6 7 8 9	12 13 14 15 17 18 19 20	9 10 11 12 13 14 15 16	I/O	Posi -tive	CPU I/F signal With parallel I/F: D0 ~ D7: bi-directional data bus With serial I/F: SP0 ~ SP5**:** common ports SCK: serial clock MOSI: serial data input See “5. CPU I/F” in detail. Regarding SP0 ~ SP5, see “11-10-1. SP0 ~ SP5 terminals” in detail.	O
INT	38	1	6	O %*	Nega -tive	CPU I/F signal Interrupt request signal output See “5. CPU I/F” and “11-8 interrupt request signal output”.	O
WRQ/MISO	39	2	7	O	Nega -tive / Posi -tive	CPU I/F signal With parallel I/F: Wait request signal (WRQ) With serial I/F: Serial data output signal (MISO) See “5. CPU I/F” in detail.	O

Terminal name	Terminal No. PCD 4611A	PCD 4621A	PCD 4641A	I/O	Logic	Description	5V tolerant
U/Bx ∗1 U/By U/Bz U/Bu	27 - - -	22 50 - -	27 36 64 73	I %	-	Select excitation method (L: unipolar / H: bipolar) See “11-6. Excitation sequence output”. They can be used as general-purpose input. See “11-9-2. U/B, F/H terminal” in detail.	O
F/Hx ∗1 F/Hy F/Hz F/Hu	28 - - -	23 51 - -	28 37 65 74	I %	-	Select excitation sequence (L: 2-2 phase / H: 1-2 phase) See “11-6. Excitation sequence output” in detail. They can be used as general-purpose input. See “11-9-2. U/B, F/H terminals” in detail.	O
STAx ∗1 STAy STAz STAu	25 - - -	24 52 - -	29 38 66 75	I %	Nega -tive	External start signal See “11-3. External start control” in detail.	O
STPx ∗1 STPy STPz STPu	26 - - -	25 53 - -	30 39 67 76	I %	Nega -tive	External stop signal See “11-4. External stop control.	O
ORGx ∗1 ORGy ORGz ORGu	18 - - -	26 54 - -	31 40 68 77	I %	Nega -tive	Origin position switch signal “11-7-3. Origin position signal” in detail.	O
+ELx ∗1 +ELy +ELz +ELy	17 - - -	27 55 - -	32 41 69 78	I %	Nega -tive	[+] direction end limit detection signal See “11-7-1. End limit detection signal” in detail.	O
-ELx ∗1 -ELy -ELz -ELu	16 - - -	28 56 - -	33 42 70 79	I %	Nega -tive	[-] direction end limit detection signal See “11-7-1 End limit detection signal” in detail.	O
+SDx ∗1 +SDy +SDz +SDu	15 - - -	29 57 - -	34 43 71 80	I %	Nega -tive	[+] direction ramping-down point detection signal See “11-7-2. Ramping-down point detection signal” in detail.	O
-SDx ∗1 -SDy -SDz -SDu	14 - - -	30 58 - -	35 44 72 81	I %	Nega -tive	[-] direction ramping-down point detection signal See “11-7-2. Ramping-down point detection signal” in detail.	O
PH1/P1x ∗1 PH1/P1y PH1/P1z PH1/P1u	30 - - -	32 41 - -	19 47 56 84	I/O %	Posi -tive	1 phase excitation output / general-purpose input / output 1 See “11-6. Excitation sequence output” and “11-9-3. U/B, F/H terminals” in detail.	O
PH2/P2x ∗1 PH2/P2y PH2/P2z PH2/P2u	31 - - -	33 42 - -	20 48 57 85	I/O %	Posi -tive	2 phase excitation output / general-purpose input / output 2 See “11-6. Excitation sequence output” and “11-9-3. P1 ~ P4 terminals” in detail.	O
PH3/P3x ∗1 PH3/P3y PH3/P3z PH3/P3u	32 - - -	34 43 - -	21 49 58 86	I/O %	Posi -tive	3 phase excitation output / general-purpose input / output 3 See “11-6. Excitation sequence output” and “11-9-3. P1 ~ P4 terminals” in detail.	O
PH4/P4x ∗1 PH4/P4y PH4/P4z PH4/P4u	33 - - -	35 44 - -	22 50 59 87	I/O %	Posi -tive	4 phase excitation output / general-purpose input / output 4 See “11-6. Excitation sequence output” and “11-9-3. P1 ~ P4 terminals” in detail.	O
+PO/PLSx∗1 +PO/PLSy +PO/PLSz +PO/PLSu	21 - - -	36 45 - -	23 51 60 88	O	-	[+] direction pulse / common pulse signal Output logic can be changed. Default is negative logic. See “11-5. Output pulse mode” in detail.	O

Terminal name	Terminal No. PCD 4611A	Terminal No. PCD 4621A	Terminal No. PCD 4641A	I/O	Logic	Description	5V tolerant
-PO/DIRx ∗1 -PO/DIRy -PO/DIRz -PO/DIRu	20 - - -	37 46 - -	24 52 61 89	O	-	[-] direction pulse / direction signal Output logic can be changed. Default is negative logic. See “11-5. Output pulse mode” in detail.	O
BSYx ∗1 BSYy BSYz BSYu	22 - - -	38 47 - -	18 46 55 83	O	Nega-tive	Running signal Running : L level output Can be used to check running status and to control motor drive current reduction while stopping.	O
OTSx ∗1 OTSy OTSz OTSu	34 - - -	39 48 - -	25 53 62 90	O	Posi-tive	General-purpose output signal See “11-9-1. OTS terminal” in detail.	O
VDD	1,19,29,37,45	3,21,40,59	5,17,45,63,91	Power	-	Power input 3.3[V] (3.0 ~ 3.6[V]) input	-
GND	10,11,12,13,24,35,40,48	11,16,31,49,61,62,63,64	8,26,54,82,93,94,95,96	Power	-	Power GND	-
(Open)	23	-	-	O	-	Output terminal for delivery inspection (always open ∗2)	-

%: Terminal that a pull-up resister is integrated

∗: Open drain terminal

∗1: Terminal names of PCD4611A do not have axis names (x).

∗2: (Open) terminal of PCD4611A is for delivery inspection. It should be always open.

4. Block diagram

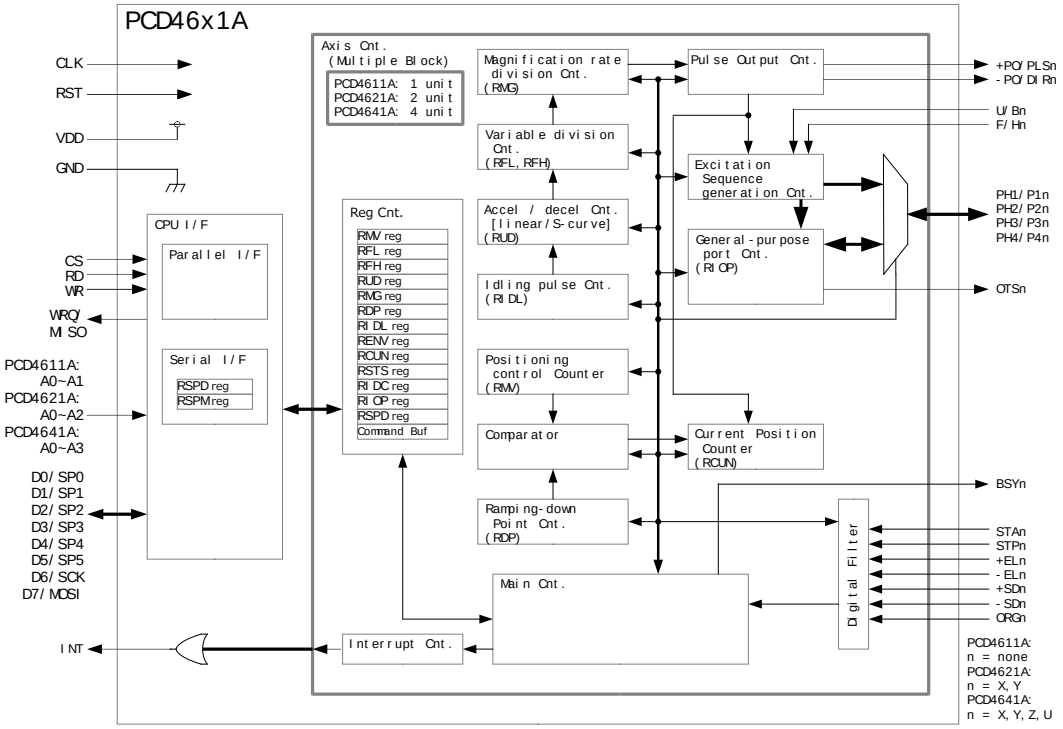


Figure 4-1 PCD46x1A block diagram

5. CPU I/F

5-1. CPU Connection

5-1-1. Outline

Select parallel I/F (8 bit) or serial I/F (synchronous 4-wire serial) for CPU I/F.
Terminals for CPU I/F can be used with both I/F.

5-1-1-1. CPU I/F signals

Table 5-1 shows CPU I/F signals list.

Table 5-1 CPU I/F signals list

Terminal	Parallel I/F		Serial I/F	
	Signal	Description	Signal	Description
CS/SS	CS	Chip selection	SS	Slave selection
WR	WR *5	Write signal	-	Not used *4
RD	RD *5	Read signal	-	Not used *4
WRQ/MISO	WRQ	Wait request	MISO	Serial data output
INT	INT	Interrupt request *3	INT	Interrupt request *3
A0/DS0	A0	Address bus bit 0	DS0	Device selection No. bit 0
A1/DS1	A1	Address bus bit 1	DS1	Device selection No. bit 1
A2 *1	A2	Address bus bit 2	-	Not used
A3 *2	A3	Address bus bit 3	-	Not used
D0/SP0	D0	Data bus bit 0	SP0	Common port 0
D1/SP1	D1	Data bus bit 1	SP1	Common port 1
D2/SP2	D2	Data bus bit 2	SP2	Common port 2
D3/SP3	D3	Data bus bit 3	SP3	Common port 3
D4/SP4	D4	Data bus bit 4	SP4	Common port 4
D5/SP5	D5	Data bus bit 5	SP5	Common port 5
D6/SCK	D6	Data bus bit 6	SCK	Serial clock
D7/MOSI	D7	Data bus bit 7	MOSI	Serial data input

*1: PCD4621A and PCD4641A have this terminal.
*2: Only PCD4641A has this terminal.
*3: There is no difference between parallel and serial.
*4: After determing CPU I/F, these terminals are not used. To determine CPU I/F, please fix these terminals to L level.
*5: In the case of use with parallel I/F, you will need external pull-up resistors in order to stabilize the initial conditions of the RD, WR terminals in high level. For detail, please see “14-1-7. Precausions in the case of use with parallel I/F”.

5-1-1-2. Selection of CPU I/F

WR and RD signal values while reset are gotten at the timing of rising reference clock and CPU I/F are set by them.
Table 5-2 shows relation between signal value during reset and CPU I/F.

Table 5-2 CPU I/F setting method

CPU I/F	Signal value during reset
Parallel I/F	Except (WR = L & RD = L)
Serial I/F	(WR = L & RD = L)

5-1-2. Parallel I/F

Table 5-3 shows the method to connect for each parallel I/F signals of PCD46x1A.

Table 5-3 Method to connect for each parallel I/F signals

Signal	Direction	Connection
CS	I	Connect with chip selection terminal of CPU
WR	I	Connect with write terminal of CPU
RD	I	Connect with read terminal of CPU
WRQ	O	Connect with wait terminal of CPU
INT	O	Connect with interrupt request terminal of CPU
A0 ~ A3	I	Connect with address bus of CPU
D0 ~ D7	I/O	Connect with data bus of CPU

Figure 5-2 shows an example of connection with CPU with parallel I/F of PCD4641A.
See “5-2. How to access with parallel I/F” for access method.

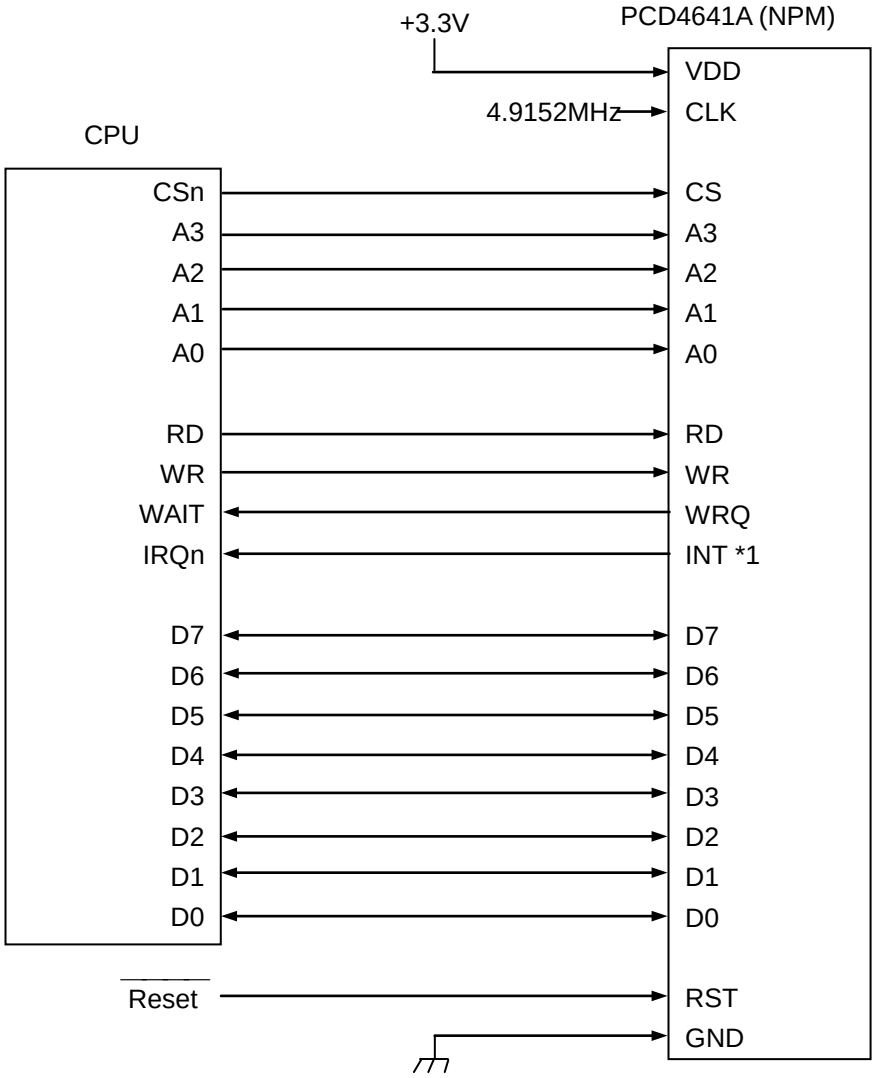


Figure 5-1 Example of parallel I/F

∗1: A pull-up resister (5k ~ 10k ohm) is needed externally.

[Note] Set the following by CPU software.

- Select “8 bit bus space” for external bus width setting.
- External wait is permitted.
- Select “L level, rising edge” for IRQ detection setting.

5-1-3. Serial I/F

Table 5-4 shows the method to connect for each serial I/F signals of PCD46x1A.

Table 5-4 Method to connect for each serial I/F signals

Signal	Direction	Connection
SS	I	Connect with slave selection terminal of CPU
SCK	I	Connect with serial clock output terminal of CPU
MOSI	I	Connect with serial data output terminal of CPU
MISO	O	Connect with serial data input terminal of CPU
INT	O	Connect with interrupt request terminal of CPU
DS0 ~ DS1	I	Set device selection No.
SP0 ~ SP5	I/O	Can be used as common ports.

This is synchronous 4-wire serial I/F.

You can access like SPI mode 0 (or 3).

With one SS signal, up to 4 LSIs can be connected.

Please assign LSI's device selection No. on the same SS signal not as to overlap the same number.

SCK clock frequency is up to 2 times of reference clock (upper limit is 15[MHz]).

Serial I/F part operates with serial clock and other circuits operate with reference clock.

Figure 5-2 shows a connection example of serial I/F of PCD46x1A with CPU.

Regarding access, see "5-3. How to access with serial I/F".

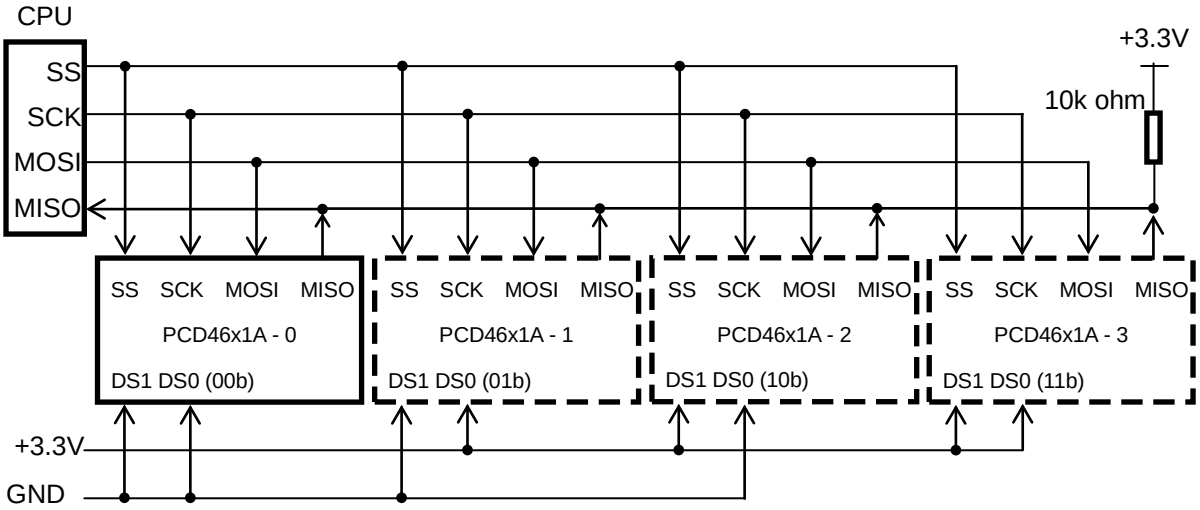


Figure 5-2 Example of serial I/F

[Note]

A pull-up resistor is connected to prevent damage from CPU or PCD46x1A at floating.

5-2. How to access with parallel I/F

5-2-1. Address map

With parallel I/F of PCD46x1A, 4-address area is occupied per axis. (1 byte per address)

Table 5-5 shows address map per axis when accessing from CPU directly.

PCD4611A is for single axis, therefore, it has 4 address areas and does not have address terminal (A3 and A2) for axis selection.

PCD4621A is for two axes, therefore, it has 8 address areas and has address terminal (A2) for axis selection to select X and Y axis.

PCD4641A is for four axes, therefore, it has 16 address areas and has address terminals (A3 and A2) for axis selection to select X, Y, Z and U axis.

Table 5-5 Address map for parallel I/F

Name	Outline
COMBF	Command buffer (8 bit) Area to write command for target axis See “6. Commands” in detail..
MSTS	Main status (8 bit) Main status area for target axis See “7-1 Main status” in detail.
RegWBF	Buffer to write to register (24 bit) Area to store write data to register When writing to bits 7 ~ 0, writes bits 23 ~ 0 data to register selected by register selection command.
RegRBF	Buffer to read out register (24 bit) Area to store read data from register Register value selected by register selection command is copied.

Table 5-6 Address map for parallel I/F per axis

A1 ~ A0	Write	Read
00b	Write to COMBF	Read out MSTS
01b	Write to RegWBF bits 7~0	Read out RegRBF bits 7~0
10b	Write to RegWBF bits 15~8	Read out RegRBF bits 15~8
11b	Write to RegWBF bits 23~16	Read out RegRBF bits 23~16

Table 5-7 Axis selection address map for parallel I/F

A3~A2	Axis	Condition
00b	X	PCD4621A (does not have A3 terminal), PCD4641A
01b	Y	PCD4621A (does not have A3 terminal), PCD4641A
10b	Z	PCD4641A only
11b	U	PCD4641A only

5-2-2. Wait control

Internal procedure to write command occurs after writing to COMBF and internal procedure to write register occurs after writing to RegWBF bits 7 ~ 0.

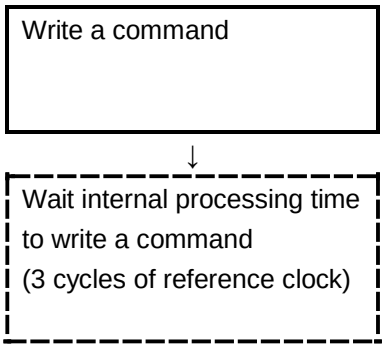
When the next access comes during internal procedure, this LSI performs wait control by outputting L level from this LSI's WRQ signal.

However, in the case of internal procedure of writing a command by writing a register select command, this LSI performs wait control only when a next access during internal procedure is Read. In the case of Write, wait control is not needed.

If your CPU does not support a WRQ signal, please use software to implement a wait time of more than 3 cycles of reference clock as internal procedure time.

5-2-3. Procedure to write a command

Figure 5-3 shows procedure to write a command.



1. Write a command to COMBF. Only when writing a register selection command, a value of the register selected is copied to RegRBF.

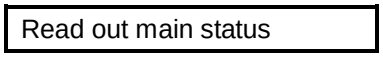
2. When WRQ output is not used, please process with software not as to access the next during internal processing.

*When WRQ signal is used this process is not needed.

Figure 5-3 Procedure to write command with parallel I/F

5-2-4. Procedure to read main status

Figure 5-4 shows procedure to read out main status.

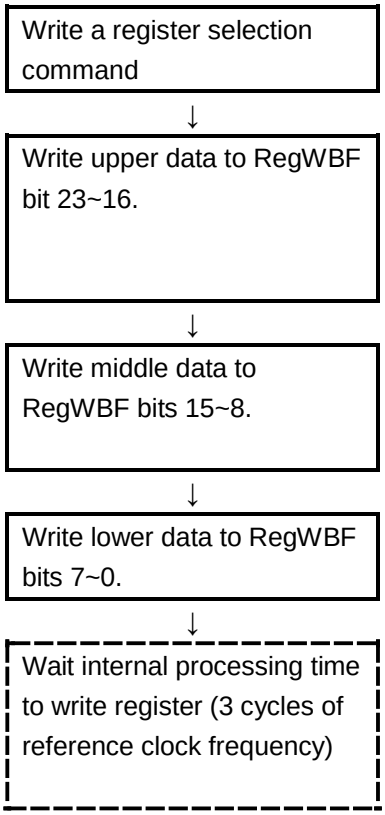


Read out MSTS.

Figure 5-4 Procedure to read out main status with parallel I/F

5-2-5. Procedure to write to a register

Figure 5-5 shows procedure to write to a register.



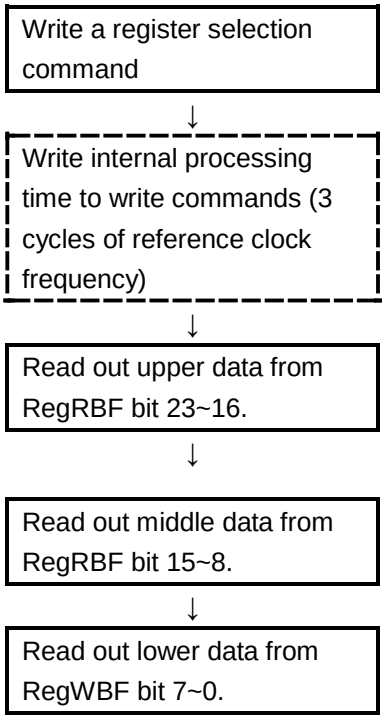
1. Write a register selection command to COMBF.
   At this time, selected register value is copied to RegRBF.
2. Write upper data.
   * This procedure is not needed for registers that has no upper data.
   * Write '00h' to RENV without fail.
3. Write middle data.
   * This procedure is not needed for registers that has no middle data.

   The order of 2 and 3 is replaceable.
4. Write lower data. Writing lower data starts batch data transfer of all bit of RegWBF.
5. When WRQ output is not used, please process with software not as to access the next during internal processing.
   *When WRQ output is used, this process is not needed.

Figure 5-5 Procedure to write to parallel I/F register

5-2-6. Procedure to read out from a register

Figure 5-6 shows procedure to read out from a register.



1. Write a register selection command to COMBF.
   At this time, selected register value is copied to RegRBF.
2. When WRQ output is not used, please process with software not as to access the next during internal processing.
   *When WRQ output is used, this process is not needed.
3. Read out data from buffer to read out registers.

In this example, the upper, middle and lower data are read in order. However, the order to read is arbitrary.

Figure 5-6 Procedure to read parallel I/F register

5-3. How to access with serial I/F

Serial I/F accesses in 8 bit unit.

Basically, as Figure 5-7 shows, the structure is as follows :Axis selection code + command + data

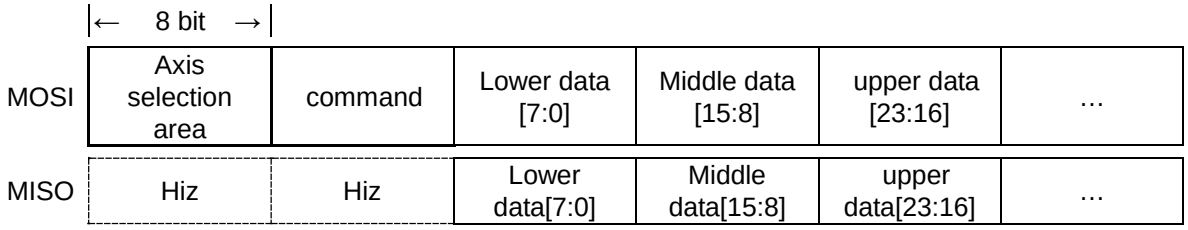


Figure 5-7 Outline of serial I/F access format

There are four access types and the type is selected by type selection area in axis selection code.

The number of bytes of command and data varies according to access type and number of axes selected.

5-3-1. Axis selection code

Access with serial I/F starts by sending axis selection code. Figure 5-8 shows structure for axis selection code.

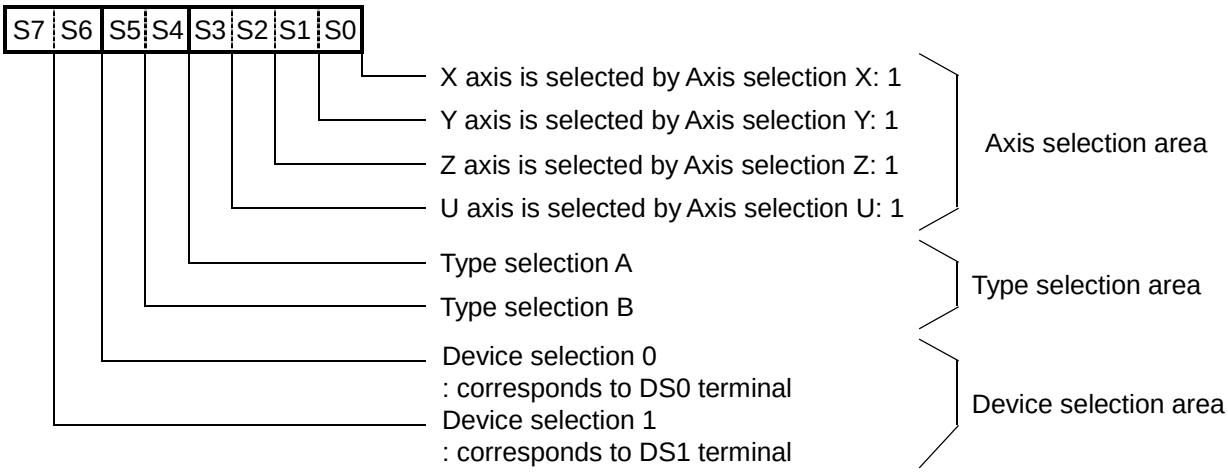


Figure 5-8 Serial I/F axis selection code

5-3-1-1. Axis selection area

Select axes to be accessed.

Axis is selected by setting the corresponding bit to '1'.

When all bit are '0', only X axis is selected.

The example that non-existent axis is selected is as follows. (Example: Y axis is selected with PCD4611A)

Write: Ignored.

Read: '0' is read out.

5-3-1-2. Type selection area

Select access type. There are four access types shown in Table 5-8.

Table 5-8 Access type with Serial I/F

Type selection		Access type	Data length
B	A		
0	0	General-purpose write operation Writes to commands and registers.	(0 ~ 24 bit) × number of axes
0	1	General-purpose read operation Reading out commands, registers and status	(24 bit) ×number of axes
1	0	Read out general-purpose port status	(8 bit) ×number of axes
1	1	Read out main status	(8 bit) ×number of axes

5-3-1-3. Device selection area

Select LSI to be accessed. Among the LSIs that the same SS signal controls, the LSIs that are consistent with Device selection No. set by DS0 and DS1 terminals are to be accessed.

If accessing to the LSI that does not consistent with, operation is as follows.

MOSI: Ignored, MISO: H level (because of pull-up)

5-3-2. General-purpose write operation

Writes to Command and Register.

Type selection is '00b'.

There are two general-purpose write operations.

- Write to Command
- Write to Register

5-3-2-1. Writing to a command

It is a method to write Start mode command, Control mode command, Register selection command, Output mode command.

See “6. Commands” for each command in detail.

It is 2 byte access.

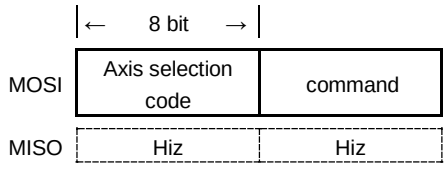


Figure 5-9 Communication format of serial I/F general-purpose write operation (write to a command)

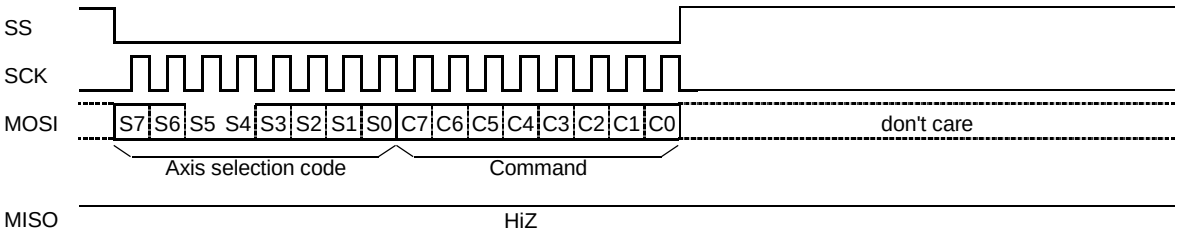


Figure 5-10 Timing of serial I/F general-purpose write operation (only command)

The timing to write a command is the rising of SS signal.

When several axes are selected, writes the same command to several axes simultaneously.

5-3-2-2. Write to a register

It is possible to write to a register by writing Register selection command to a command and by sending data in order of lower, middle and upper.

See “6-3. Register selection command” for Register selection command in detail.

When several axes are selected, send selected axes data in order of lower, middle and upper.

For example, Y and U axes are selected, send Y axis data (in order of lower, middle and upper data) and U axis data (in order of lower, middle and upper data).

It is 2 + (3 x number of axes) byte access.

MOSI	Axis selection code	command	Lower data [7:0]	Middle data [15:8]	Upper data [23:16]	…
MISO	Hiz	Hiz	Hiz	Hiz	Hiz	…

Figure 5-11 Communication format of serial I/F general-purpose write operation (write to a register)

The timing to write to Register is the rising of SS signal.

[Note] The number of data varies according to whether the number of axes is single or plural. If single axis is selected, it is possible to omit writing data to registers that have no middle data and upper data. If several axes are selected, send the selected axes data multiplying by 24 bit data. The border of write data is determined per 24-bit. Although non-existent bits are ignored, send “0” for future extension.

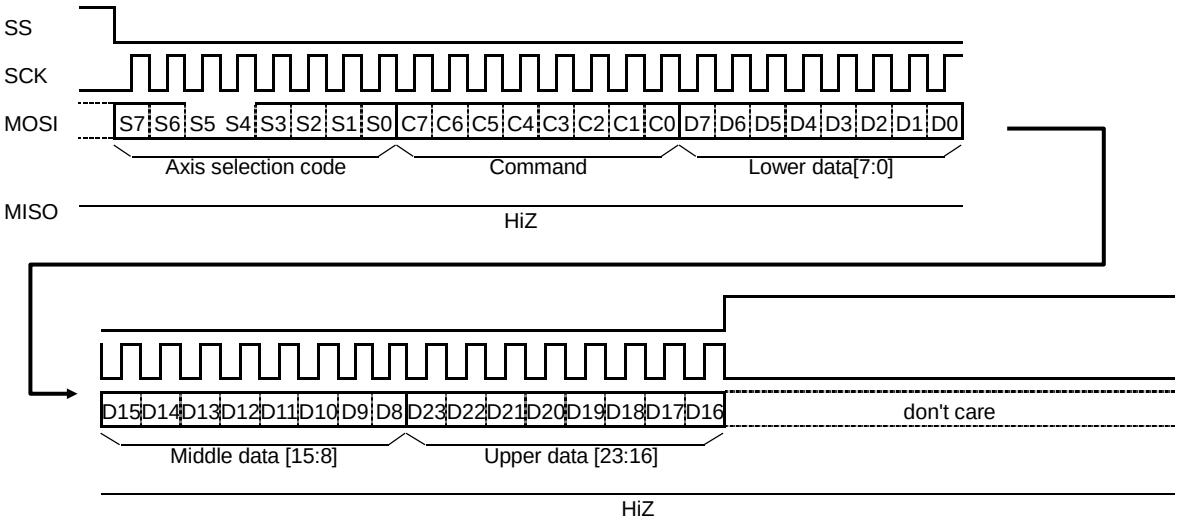


Figure 5-12 Timing of serial I/F general-purpose write operation (write to a register)

An example of several axes selected is described in appendix A.

Writing to RSPO and RSPM registers that there is one in the LSI is different from writing to other registers.

Sending data in axis selection area is ignored. (Send arbitrary data.)

It is 3 byte access.

MOSI	Axis selection code	Command	Data [7:0]
MISO	Hiz	Hiz	Hiz

Figure 5-13 Communication format of serial I/F general-purpose write operation (Write to RSPO and RSPM registers)

Access is complete by 3 bytes.

All accesses are ignored until the following SS rises.

The timing to write to Registers is just after the third byte of access is complete to send. This access is dealt regardless of whether SS rise to high or not.

5-3-3. General-purpose read operation

Read commands, status and registers. Type selection is '01b'. A command following Axis selection code is different from one of general-purpose write operation. Table 5-9 shows these commands. When several axes are selected, read data for selected axes are outputs in order of X axis, Y axis, Z axis and U axis.

Table 5-9 Serial I/F general-purpose read command

Read command		Operation
Upper 4 bits	Lower 4 bits	
0000b	0000b	Read out a command Read out Start mode command, Control mode command and Register selection command
0001b	0000b	Read out status Read out main status and extended status
0010b ～ 0111b	-	Undefined commands Do not use them.
1000b	SSSSb	Read out register Read out registers by selecting register selection code (Table 8-4) with "SSSS". Corresponds to RCM3 ~ 0.
1001b ～ 1111b	-	Undefined commands Do not use them.

5-3-3-1. Read out a command

Outputs read data in order of Start mode command, Control mode command and Register selection command. Read command is '00h'.

It is 2 + (3 × the number of axes) byte access.

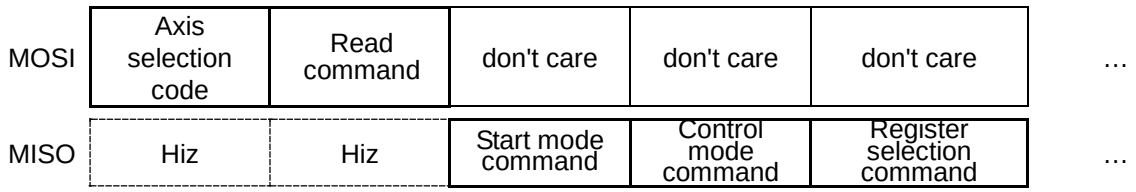


Figure 5-14 Communication format of serial I/F general-purpose read operation (Read a command)

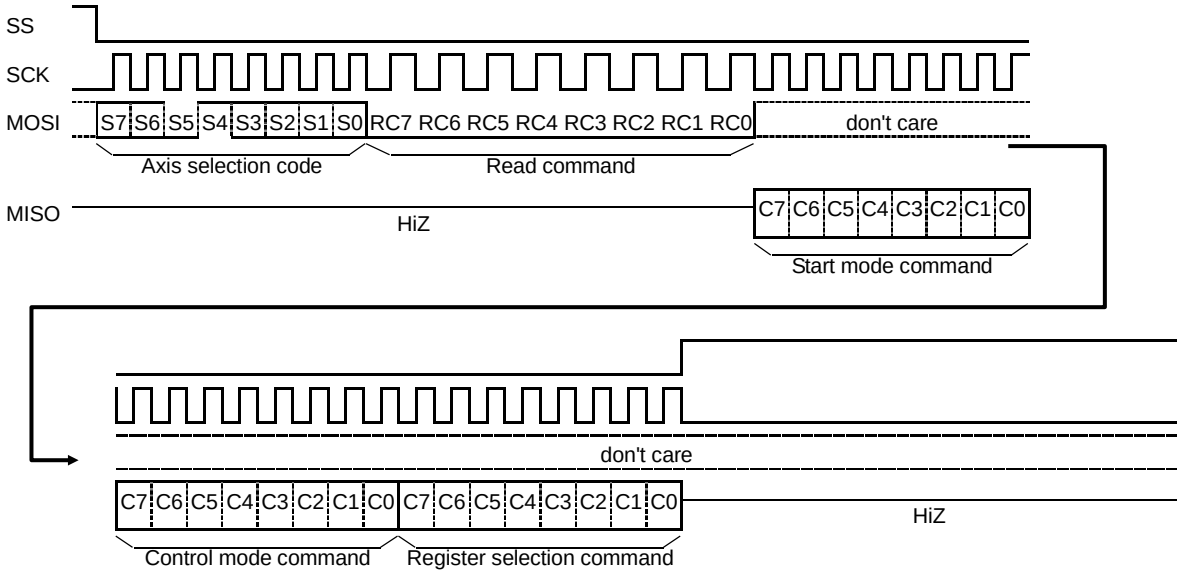


Figure 5-15 Timing of serial I/F general-purpose read operation (Read a command)

When several axes are selected in axis selection area, read data of Start mode command, Control mode command and Register selection command for all axes selected are output.

Just after writing bit 6 of read command, Start mode command, Control mode command and Register selection command of all axes are latched simultaneously and read out.

When you want to read out Output mode command, read them as upper data of RMG register with reading registers.

The access example when several axes are selected are shown in “Appendix A”.

5-3-3-2. Read out status

Outputs read data in order of main status (MSTS), Lower data (RSTS bit 7 ~ 0) of extended status and Middle data (RSTS bits 15 ~ 8) of extended status. Read command is '10h'.

It is 2 + (3 × number of axes) byte access.

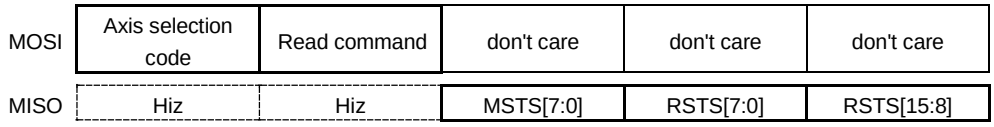


Figure 5-16 Communication format of serial I/F general-purpose read operation (Read out status)

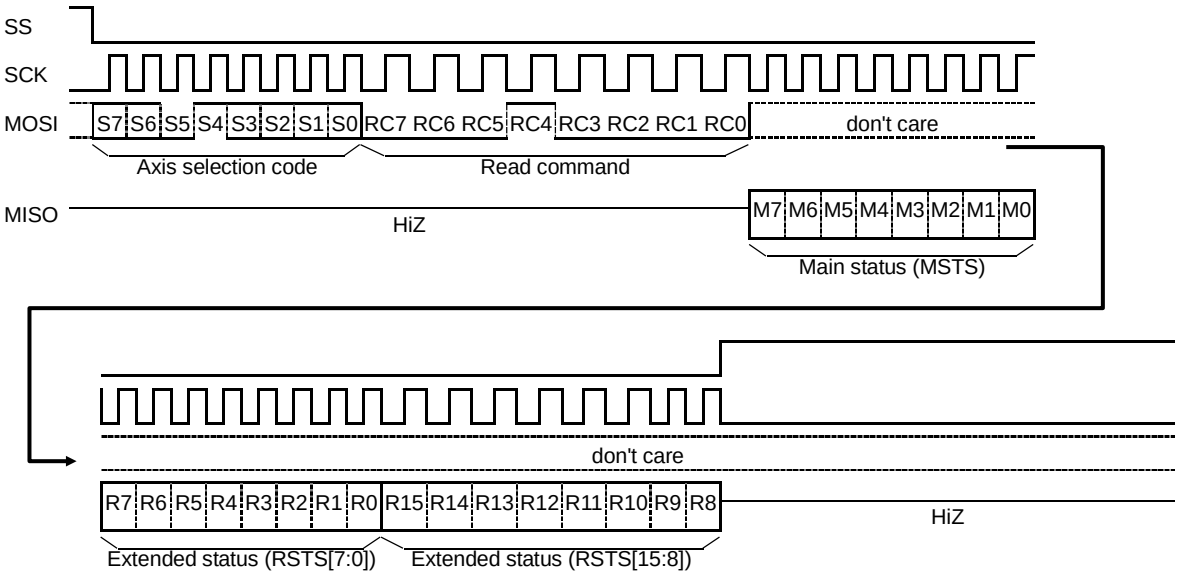


Figure 5-17 Timing of serial I/F general-purpose read operation (Read out status)

When several axes are selected in axis selection area, status for all axes selected are output.

Just after writing bit 6 of read command, Start mode command, Control mode command and Register selection command of all axes are latched simultaneously and read out.

The access example when several axes are selected is shown in “Appendix A”.

5-3-3-3. Read out register

The LSI outputs read data in the order of lower data (bits 7 ~ 0), middle data (bits 15 ~ 8), upper data (bits 23 ~ 16) of register data.

Read command is '1000_SSSSb'. Select register selection code (Table 8-4) by 'SSSS'.

It is 2 + (3 × number of axes) byte access.

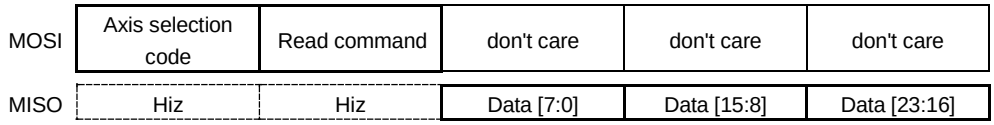


Figure 5-18 Communication format of serial I/F general-purpose read operation (Read out a register)

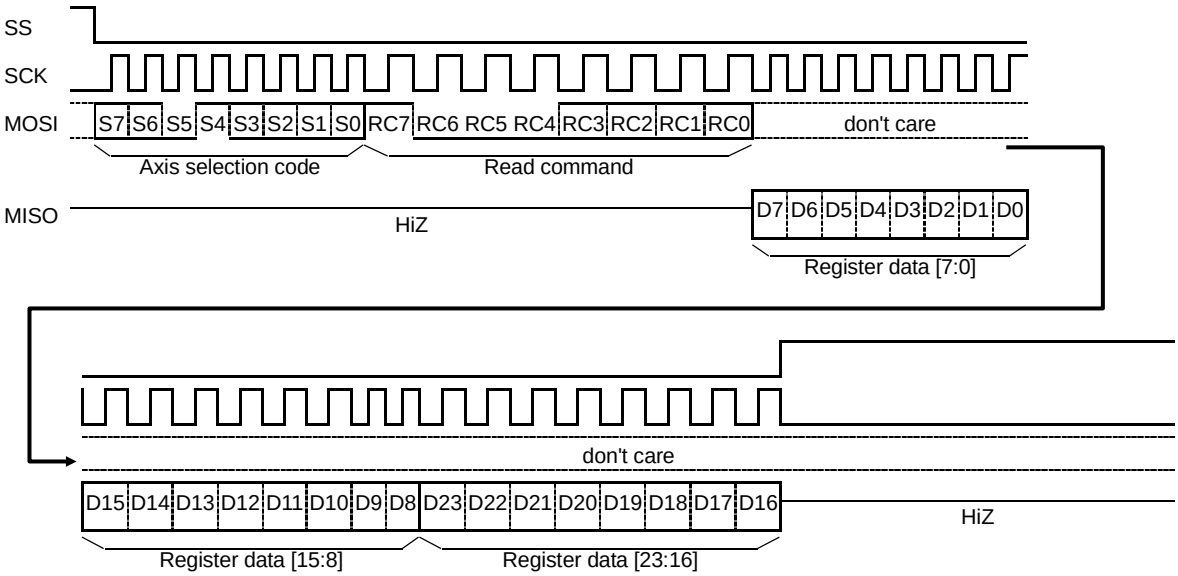


Figure 5-19 Timing of serial I/F general-purpose read operation (register read out)

When several axes are selected, the LSI outputs register data of the same register selection of all selected axis. Just after bit 2 of read command is written, register of all axes are latched simultaneously and the LSI outputs them. Even if the case that there are no middle data and upper data, it is needed to read 24 bits.

The access example when several axes are selected is shown in “Appendix A”.

Read operation for RSPO and RSPM register that there is one in one LSI is different from read operation of other registers.

Sending data is ignored in axis selection area. (Please send arbitrary data.)

The receiving data is only 8 bit.

Read command is “1000_SSSSb'. Select 'SSSS' register selection code (Table 8-4) with 'SSSS'.

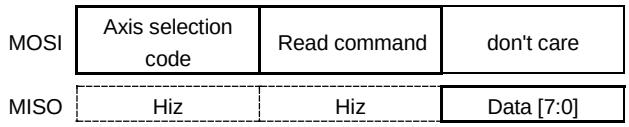


Figure 5-20 Communication format of serial I/F general-purpose read operation (Read out RSPO and RSPM register)

5-3-4. Read out general-purpose port status

The LSI reads out general-purpose port status for each axis.

Register value in RENV.IOPM and RIOP (bits 5 ~ 0) can be checked.

Type selection is '10b'.

Any commands are not needed.

When several axes are selected, data is output in order of X axis, Y axis, Z axis and U axis.

It is 1 + (1 x number of axis) byte access.

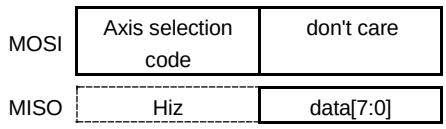


Figure 5-21 Communication format of serial I/F general-purpose port status read out operation

Table 5-10 Read data of serial I/F general-purpose port status read out operation

Bit	Bit name	Description
0	P0	RIOP.CP1 value
1	P1	RIOP.CP2 value
2	P2	RIOP.CP3 value
3	P3	RIOP.CP4 value
4	P4	RIOP.MUB value
5	P5	RIOP.MFH value
6	Undefined	(Always '0')
7	EN	RENV.IOPM value

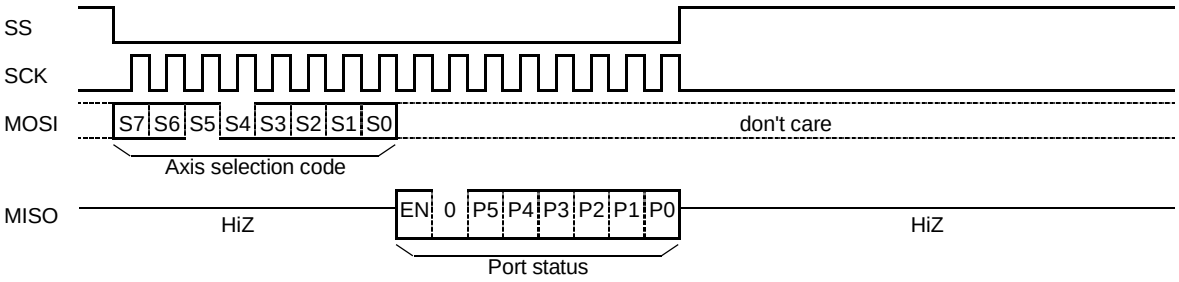


Figure 5-22 Timing of serial I/F general-purpose port status read out

When several axes are selected in axis selection area, all selected axes' general-purpose port status is read out. Just after bit 4 of axis selection code is written, all axes' general-purpose port status is latched simultaneously and read out.

The access example when several axes are selected is shown in “Appendix A”.

5-3-5. Read out main status

Reads out each axis' main status.

Type selection is '11b'.

Any commands are needed.

When several axes are selected, data of selected axis can be read in order of X axis, Y axis, Z axis, U axis.

Its access is 1 + (1 × number of axes) byte one.

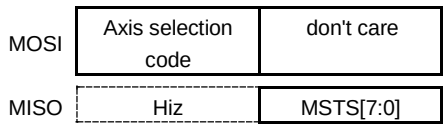


Figure 5-23 Communication format of serial I/F main status read out operation

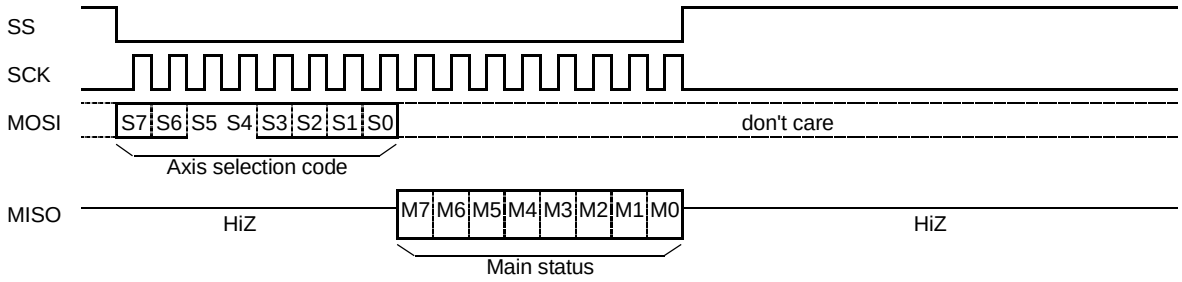


Figure 5-24 The timing of serial I/F main status read operation

When several axes are selected in axis selection area, all selected axes' general-purpose port status is read out. Just after bit 4 of axis selection code is written, all axes' general-purpose port status is latched simultaneously and read out.

The access example when several axes are selected is shown in “Appendix A”.

6. Commands

Commands to control this LSI are written in 8-bit to command buffer (COMBF).

Written commands are classified in the following four type by value of the upper 2 bits and stored.

Table 6-1 Command type

Bit 7 and 6	Command type
00b	Start mode command FL constant speed start, FH constant speed start, high speed (with acceleration / deceleration) start, immediate stop, deceleration and stop and stop command.
01b	Control mode command Commands regarding operation mode such as continuous operation, origin return operation and positioning operation.
10b	Register selection command Commands to select a target register when writing to and reading out internal register.
11b	Output mode command Commands regarding setting of input / output signals such as output pulse logic, mask of sequence output, applying to a filter and selection of monitor mode.

Note 1. Operation starts by writing start mode command
Write control mode command, output mode command and set register for operation and write Start mode command.

Note 2. If you want the same setting of Control mode command and Output mode command as the previous time, re-writing is not needed.

Note 3. If you want the same setting of register other than RMV register as the previous time,re- writing is not needed.

Note 4. Even if the same feeding amount of positioning operation is repeated, please write a feeding amount to RMV register every time.

6-1. Start mode command

It is a command about start / stop.

Table 6-2 Bit name of start mode command

7	6	5	4	3	2	1	0
0	0	SCM5	SCM4	SCM3	SCM2	SCM1	SCM0

Table 6-3 Description of start mode command

Bit	Bit name	Description
0	SCM0	Operation speed selection 0: Run at FL speed (RFL setting speed) 1: Run at FH speed (RFH setting speed)
1	SCM1	Hold start control 0: Normal start 1: Hold start and start by STA signal input.
2	SCM2	Speed mode selection 0: Constant speed operation 1: High speed (with acceleration / deceleration) operation
4~3	SCM4~3	Start / Stop control 01: Request to stop immediately 10: Request to start 11: Request to decelerate and stop ∗1
5	SCM5	INT output control when a motor stops 0: Does not output INT signal when a motor stops. (INT factor is cleared) 1: Outputs INT signal when a motor stops.

∗1: To request deceleration and stop, set SCM2 to “1” High speed (with acceleration / deceleration) operation).

Table 6-4 Start mode command List

Start mode command		Operation description
Bits 7 ~ 0	Hex	
0001_0000b	10h	FL constant speed start (No INT occurs at stopping / The factor is cleared.) If this command is written while a motor stops, the motor starts constant operation at FL speed. If this command is written while a motor runs, speed is changed to FL speed immediately
0011_0000b	30h	FL constant speed start (INT occurs at stopping)
0001_0010b	12h	FL constant speed hold start (No INT at stopping / The factor is cleared.)
0011_0010b	32h	FL constant speed hold start (INT occurs at stopping)
0001_0001b	11h	FH constant speed start (No INT at stopping / The factor is cleared.) If this command is written while a motor stops, the motor starts constant operation at FH speed. If this command is written while a motor runs, the speed is changed to FH speed immediately.
0011_0001b	31h	FH constant speed start (INT occurs at stopping)
0001_0011b	13h	FH constant speed hold start (No INT at stopping / The factor is cleared)
0011_0011b	33h	FH constant speed start hold (INT occurs at stopping)
0001_0101b	15h	FH High speed start (No INT at stopping / The factor is cleared.) If this command is written while a motor stops, a motor starts at FL speed and accelerate to FH speed. If this command is written while a motor is running, a motor starts to accelerate to FH speed.
0011_0101b	35h	FH high speed start (INT occurs at stopping)
0001_0111b	17h	FH high speed hold start (No INT at stopping / The factor is cleared.)
0011_0111b	37h	FH high speed start hold (INT occurs at stopping)
0001_0100b	14h	Deceleration on the way (No INT at stopping / The factor is cleared.) If this command is written while a motor runs, the motor decelerates to FL speed. If this command is written while a motor runs, the motor starts constant operation at FL speed.
0011_0100b	34h	Deceleration on the way (INT occurs at stopping)
0001_1101b	1Dh	Decelerate and stop (INT occurs at stopping / The factor is cleared.) When this command is written during the motor is running at FH speed, operation decelerates to FL speed and stops. When this command is written while a motor is running at FL speed, a motor stops immediately.
0011_1101b	3Dh	Decelerate and stop (INT occurs at stopping)
0000_1000b	08h	Stop immediately (No INT occurs at stopping / The factor is cleared.)
0010_1000b	28h	Stop immediately (INT occurs at stopping)
00X1_1X1Xb	-	Prohibited setting

[Note] The maximum time from writing an immediate stop command to stop (BSY = H level) is FL pulse cycle.

6-2. Control mode command

These are commands regarding operation mode mode.

Table 6-5 Bit names of control mode command

7	6	5	4	3	2	1	0
0	1	CCM5	CCM4	CCM3	CCM2	CCM1	CCM0

Table 6-6 Description of control mode command

Bit	Bit name	Description
0	CCM0	ORG signal control 0: Ignores ORG input. 1: When ORG input becomes L level, operation stops immediately or decelerates and stops. RENV.ORDS is used to select immediate stop or deceleration and stop.
1	CCM1	+SD, -SD signal control 0: Ignores +SD, -SD input. 1: When SD signal of the same direction as operation becomes L level, operation decelerates to FL speed.
2	CCM2	Positioning operation control 0: Operation is not affected by the RMV setting value. (Continuous operation mode) 1: Pulses set in the RMV are outputs and the motor stops automatically. (Positioning mode)
3	CCM3	Select operation direction 0: Operation direction becomes [+] direction. 1: Operation direction becomes [-] direction.
4	CCM4	OTS output signal control 0: OTS terminal output goes L level. 1: OTS terminal output goes H level.
5	CCM5	Acceleration / deceleration characteristics control 0: Acceleration / deceleration characteristics become linear. 1: Acceleration / deceleration characteristics become S-curve.

6-3. Register selection command

This is a command to select registers to write to or read out mainly.

Table 6-7 Bit names of register selection command

7	6	5	4	3	2	1	0
1	0	RCM5	RCM4	RCM3	RCM2	RCM1	RCM0

Table 6-8 Description of Register selection command

Bit	Bit name	Description
2~0	RCM2~0	Register selection code PCD46x1 mode: Select registers to write to or read out with 4 bits in RCM3~0. Other mode: Select registers to write or read out with 3 bits in RCM2~0. For detail, see “8. Register”.
3	RCM3	Register selection code (for PCD46x1 mode) Selects registers to write to or read out with 4 bits in RCM3~0. Down counter operation control for positioning control is set by the setting of RENV.DCSP.
		Down count operation control for positioning control (When RENV.46MD = 0) 0: Down count by output pulse. (Normal operation) 1: Stop count (pulses are output) This setting has priority and the setting of RENV.DCSP becomes disabled.
4	RCM4	Interrupt output control when passing ramping-down point 0:INT signals are not output when passing ramping-down point (The INT factor is cleared) 1: INT signal are output when passing a ramping-down point.
5	RCM5	External start interrupt output control 0: An INT signal is not output even if starting by STA input. (This INT factor is cleared.) 1: An INT signal is output when starting by STA input.

6-4. Output mode command

These are commands about input / output signal.

Table 6-9 Bit names of output mode command

7	6	5	4	3	2	1	0
1	1	OCM5	OCM4	OCM3	OCM2	OCM1	OCM0

Table 6-10 Description of output mode command

Bit	Bit name	Description
0	OCM0	+PO/PLS, -PO/DIR output logic setting 0: +PO, -PO and PLS are negative logic pulse. DIR is H level at [+] direction. 1: +PO, -PO and PLS are positive logic pulse. DIR is L level at [+] direction.
1	OCM1	Pulse output mask control 0: Pulses are output while a motor is running. (Normal operation) 1: Pulses output are masked and sequence output change stops. (Current position counter is operating.)
2	OCM2	Excitation sequence output mask control 0: Sequence signals are output. (Normal operation) 1: Sequence signals output are masked. (Fixed value is output.) Output of fixed value when masked is set by RENV.MSKM. When RENV.IOPM = 1, sequence output terminal is a general-purpose port terminal. Terminal status is not changed by this setting. (RSTS.SPH1~SPH4 are changed.)
3	OCM3	Stop control during acceleration / deceleration operation 0: Acceleration and deceleration is available (Normal acceleration and deceleration) 1: Acceleration and deceleration stop on the way (fixed to a speed on the way during acceleration or deceleration.) Making this bit to 1 while acceleration and deceleration keeps the speed at the time and making this bit to 0 cancels keeping the speed.
4	OCM4	Applying ORG, +EL, -EL, STP signal filter 0: No filter 1: With filter (responds to longer than 3 cycle width pulse input of reference clock.)
5	OCM5	Select monitor mode 0: Standard monitor mode (PCD4500 compatible mode) ∗1 1: Extended monitor mode (recommended) (PCD45x1compatible mode ∗1 or PCD46x1 mode (selected by RENV.46MD)) With Serial I/F, fixed to '1. ('0' is ignored though it is written.)

∗1: This mode is compatible with old products (PCD4500 and PCD45x1). Use PCD46x1 mode if you do not need this compatibility.

7. Status

7-1. Main status

Main status (MSTS) monitor.

With parallel I/F, refer to “5-2-4. Procedure to read main status”.

With serial I/F, refer to “5-3-3-2. Read out status / 5-3-5. Read out main status”

Table 7-1 Bit names of Main status

7	6	5	4	3	2	1	0
FDWN	FUP	SDP	PLSZ	BUSY	ISTA	ISDP	ISTP

Table 7-2 Description of main status

Bit	Bit name	Description
0	ISTP	Requesting an interrupt by stop 0: ON 1: OFF
1	ISDP	Requesting an interrupt at passing a ramping-down point. 0: ON 1: OFF
2	ISTA	External start interrupt request 0: ON 1: OFF
3	BUSY	Operation status monitor 0: Stopping 1: Running
4	PLSZ	Remaining pulse 0 monitor 1: RMV = 0
5	SDP	Monitor at passing a ramping-down point 1: RMV ≤ RDP
6	FUP	Acceleration status monitor 1: Accelerating
7	FDWN	Deceleration status monitor 1: Decelerating

7-2. Extended status

Extended status (RSTS) monitor.

With parallel I/F, refer to “5-2-6. Procedure to read out register (RSTS)”

With serial I/F, refer to “5-3-3-2. Read out status / 5-3-2-2 Read out register (RSTS)”

Table 7-3 Bit names of extended status

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SINT	SOTS	SPPO	SMPO	SPH4	SPH3	SPH2	SPH1	SPHZ	SPSD	SMSD	SSTA	SSTP	SORG	SPEL	SMEL

Table 7-4 Description of extended status

Bit	Bit name	Description
0	SMEL	-EL terminal status monitor 0: OFF status (H level) 1: ON status (L level)
1	SPEL	+EL terminal status monitor 0: OFF status (H level) 1: ON status (L level)
2	SORG	ORG terminal status monitor 0: OFF status (H level) 1: ON status (L level)
3	SSTP	STP terminal status monitor 0: OFF status (H level) 1: ON status (L level)
4	SSTA	STA terminal status monitor 0: OFF status (H level) 1: ON status (L level)
5	SMSD	-SD terminal status monitor 0: OFF status (H level) 1: ON status (L level)
6	SPSD	+SD terminal status monitor 0: OFF status (H level) 1: ON status (L level)
7	SPHZ	Excitation origin position monitor (refer to “11-6. Excitation sequence output”) 1: Excitation origin position
8	SPH1	PH1 signal monitor 0: L level 1: H level
9	SPH2	PH2 signal monitor 0: L level 1: H level
10	SPH3	PH3 signal monitor 0: L level 1: H level
11	SPH4	PH4 signal monitor 0: L level 1: H level
12	SMPO	-PO/DIR signal monitor 0: L level 1: H level
13	SPPO	+PO/PLS signal monitor 0: L level 1: H level
14	SPTS	OTS signal monitor 0: L level 1: H level
15	SINT	Interrupt request status monitor (per axis) 0: OFF status 1: ON status

7-3. Product information code

Production information code (RIDC) monitor.

With parallel I/F, refer to “5-2-6. Procedure to read out register (RIDC)” to check product information code.

With serial I/F, refer to “5-3-2-2. Read out register (RIDC)” to check product information code.

Table 7-5 Bit name to monitor Product information code

7	6	5	4	3	2	1	0
IDC3	IDC2	IDC1	IDC0	VRC	0	0	S46M

Table 7-6 Description of production code monitor

Bit	Bit name	Description
0	S46M	Monitor of a value in RENV.46MD
2~1	Undefined	(Always '00b')
3	VRC	Version discriminant code In PCD46x1A, always ‘1’. 0: PCD46x1 (Old version) 1: PCD46x1A
7~4	IDC3~0	Product information code 1001b: 1-axis (PCD4611A) 1010b: 2-axis (PCD4621A) 1100b: 4-axis (PCD4641A)

8. Register

8-1. Register list

There are the following registers per axis in PCD46x1A. (There are one RSPO and one RSPM per LSI)
According to the setting of compatible mode, accessible registers are changeable.
With serial I/F, mode is fixed to the PCD46x1 mode.

Table 8-1 Register list

Register name	Description	Bit length	Setting range	Accessible/inaccessible by compatible mode		
				PCD 46x1	PCD 45x1	PCD 4500
RMV	Preset feed amount / confirm remaining pulses	24	0 ~ 16,777,215	R/W	R/W	R/W
RFL	Set FL speed	13	1 ~ 8,191	R/W	R/W	W
RFH	Set FH speed	13	1 ~ 8,191	R/W	R/W	W
RUD	Set acceleration / deceleration rate	16	1 ~ 65,535	R/W	R/W	W
RMG	Set magnification	10	2 ~ 1,023	R/W	R/W	W
RDP	Set ramping-down point	24	0 ~ 16,777,215 or -8,388,608 ~ +8,388,607	R/W	R/W	W
RIDL	Set idling pulses	3	0 ~ 7	R/W	R/W	W
RENV	Set environmental data	16	0000h ~ FFFFh	R/W	R/W	W
RCUN	Current position counter	24	0 ~ 16,777,215 or -8,388,608 ~ +8,388,607	R/W	-	-
RSTS	Extended status	16	0000h ~ FFFFh	R	R	-
RIDC	Product information code	8	00h ~ FFh	R	R	-
RIOP	Set general-purpose ports	6	00h ~ 3Fh	R/W	-	-
RSPD	Current speed monitor	13	0 ~ 8,191	R	-	-
RSPO	Common port output control / monitor	6	0h ~ 3Fh	R/W *	-	-
RSPM	Common port attribute setting	6	0h ~ 3Fh	R/W *	-	-

R/W: Both reading and writing are possible
*: Only with serial I/F, one per LSI
W : Only writing.
R : Only reading.
- : Access impossible

8-2. Compatible mode setting

PCD46x1A is compatible with our old product PCD4500 series.
By Output mode command.OCM5 and RENV.46MD, compatible mode can be switched by RENV.46MD.
When switching from default status to compatible mode, set in order of output mode command and environmental setting register.
With serial I/F, mode is fixed to PCD46x1 mode.
To learn about the difference from our product, refer to Appendix B. Difference from PCD45x1.

Table 8-2 Compatible mode setting

OCM5	46MD	Compatible mode name
1	1	PCD46x1 mode (Recommended)
1	0	PCD45x1 compatible mode
0	1	Setting is prohibited
0	0	PCD4500 compatible mode (Default)

[Difference from PCD4500 series]

Note 1. Among RENV registers added to PCD4600 series, RENV register can be used in PCD45x1 compatible mode and PCD4500 compatible mode.

Note 2. Register width of acceleration / deceleration rate setting (RUD) register is extended from 10 bit to 16 bit and register length of ramping-down point setting (RDP) is extended from 16 bit to 24 bit in PCD45x1 compatible mode and PCD4500 compatible mode. When you use the extended bits in software for PCD4500 and PCD45x1, please confirm that extended bit is “0” when writing to a register.

8-2-1. PCD46x1 mode

This is a mode to access all registers of PCD46x1A.

It has 4 bits space (RCM3~ 0) of Register selection command.

Table 8-3 PCD46x1 mode register selection code (When writing)

RCM3 ~ 0	RegWBF		
	Upper data (bits 23~16)	Middle data (bits 15~8)	Lower data (bits 7~0)
0000b	RMV (bits 23~16)	RMV (bits 15~8)	RMV (bits 7~0)
0001b	(Disabled)	RFL (bits 15~8)	RFL (bits 7~0)
0010b	(Disabled)	RFH (bits 15~8)	RFH (bits 7~0)
0011b	(Disabled)	RUD (bits 15~8)	RUD (bits 7~0)
0100b	(Disabled)	RMG (bits 15~8)	RMG (bits 7~0)
0101b	RDP (bits 23~16)	RDP (bits 15~8)	RDP (bits 7~0)
0110b	(Disabled)	(Disabled)	RIDL (bits 7~0)
0111b	00h ※1	RENV (bits 15~8)	RENV (bits 7~0)
1000b	RCUN (bits 23~16)	RCUN (bits 15~8)	RCUN (bits 7~0)
1001b	(Disabled)	(Disabled)	(Disabled)
1010b	(Disabled)	(Disabled)	RIOP (bits 7~0)
1011b	(Disabled)	(Disabled)	RSPO (bits 7~0) ∗2
1100b	(Disabled)	(Disabled)	RSPM (bits 7~0) ∗2
1101b	Access is prohibited.		
1110b			
1111b			

The area with (Disabled) should be written to '00h' for future extension.

∗1: Make sure to write 00h in the RENV (bits 23 ~ 16) for delivery inspection.

∗2: This is a register to be accessible with serial I/F only.

Table 8-4 PCD46x1 mode register selection code (When Reading)

RCM3 ~ 0	RegRBF		
	Upper data (Bits 23~16)	Middle data (Bits 15~8)	Lower data (Bits 7~0)
0000b	RMV (Bits 23~16)	RMV (Bits 15~8)	RMV (Bits 7~0)
0001b	Start mode command	RFL (Bits 15~8)	RFL (Bits 7~0)
0010b	Control mode command	RFH (Bits 15~8)	RFH (Bits 7~0)
0011b	Register selection command	RUD (Bits 15~8)	RUD (Bits 7~0)
0100b	Output mode command	RMG (Bits 15~8)	RMG (Bits 7~0)
0101b	RDP (Bits 23~16)	RDP (Bits 15~8)	RDP (Bits 7~0)
0110b	RSPD (Bits 15~8)	RSPD (Bits 7~0)	RIDL (Bits 7~0)
0111b	RIDC (Bits 7~0)	RENV (Bits 15~8)	RENV (Bits ~0)
1000b	RCUN (Bits 23~16)	RCUN (Bits 15~8)	RCUN (Bits 7~0)
1001b	00h	RSTS (Bits 15~8)	RSTS (Bits 7~0)
1010b	00h	00h	RIOP (Bits 7~0)
1011b	00h	00h	RSPO (Bits 7~0) ∗1
1100b	00h	00h	RSPM (Bits 7~0) ∗1
1101b	00h	00h	00h
1110b	00h	00h	00h
1111b	00h	00h	00h

∗1: This is a register to be accessible only with serial I/F. ('00h' with parallel I/F)

8-2-2. PCD45x1 compatible mode

This mode is compatible with PCD45x1.

It has 3 bits space (RCM2 ~ 0) of Register selection command

Table 8-5 Register selection code of PCD45x1 compatible mode and PCD4500 compatible mode (When writing)

RCM2 ~ 0	RegWBF		
	Upper data (Bits 23~16)	Middle data (Bits 15~8)	Lower data (Bits 7~0)
000b	RMV (Bits 23~16)	RMV (Bits 15~8)	RMV (Bits 7~0)
001b	(Disabled)	RFL (Bits 15~8)	RFL (Bits 7~0)
010b	(Disabled)	RFH (Bits 15~8)	RFH (Bits 7~0)
011b	(Disabled)	RUD (Bits 15~8)	RUD (Bits 7~0)
100b	(Disabled)	RMG (Bits 15~8)	RMG (Bits 7~0)
101b	RDP (Bits 23~16)	RDP (Bits 15~8)	RDP (Bits 7~0)
110b	(Disabled)	(Disabled)	RIDL (Bits 7~0)
111b	00h ∗1	RENV (Bits 15~8) ∗2	RENV (Bits 7~0) ∗2

The area with (Disabled) should be written to '00h' for future extension.

∗1: Make sure to write 00h in the RENV (bits 23 ~ 16) for delivery inspection.

∗2: PCD4511 and PCD4521 do not have RENV register and PCD4541 has only 1 bit.

16 bit can be used in PCD45x1 compatible mode and PCD4500 compatible mode of PCD46x1A.

Table 8-6 Register selection code of PCD45x1 compatible mode (When reading)

RCM2 ~ 0	RegRBF		
	Upper data (Bits 23~16)	Middle data (Bits 15~8)	Lower data (Bits 7~0)
000b	RMV (Bits 23~16)	RMV (Bits 15~8)	RMV (Bits 7~0)
001b	Start mode command	RFL (Bits 15~8)	RFL (Bits 7~0)
010b	Control mode command	RFH (Bits 15~8)	RFH (Bits 7~0)
011b	Register selection command	RUD (Bits 15~8)	RUD (Bits 7~0)
100b	Output mode command	RMG (Bits 15~8)	RMG (Bits 7~0)
101b	RENV (Bits 7~0)	RDP (Bits 15~8)	RDP (Bits 7~0)
110b	RSPD (Bits 15~8)	RSPD (Bits 7~0)	RIDL (Bits 7~0)
111b	RIDC (Bits 7~0)	RSTS (Bits 15~8)	RSTS (Bits 7~0)

8-2-3. PCD4500 compatible mode

This is a mode that is compatible with PCD4500.

It has 3-bit space of RCM2 ~ 0 of register selection command.

At writing, it is the same as PCD45x1 compatible mode.

Table 8-7 Register selection code of PCD4500 compatible mode (When reading)

RCM2 ~ 0	RegRBF		
	Upper data (Bits 23~16)	Middle data (Bits 15~8)	Lower data (Bits 7~0)
000b	RMV (Bits 23~16)	RMV (Bits 15~8)	RMV (Bits 7~0)
001b	00h	00h	RSTS (Bits 7~0)
010b	00h	00h	RSTS (Bits 7~0)
011b	00h	00h	RSTS (Bits 7~0)
100b	00h	00h	RSTS (Bits 7~0)
101b	00h	00h	RSTS (Bits 7~0)
110b	00h	00h	RSTS (Bits 7~0)
111b	00h	00h	RSTS (Bits 7~0)

8-3. Register details

8-3-1. RMV

This is a 24-bit register to set number of output pulse in positioning operation mode.
The setting range is 0 (000000h) ~ 16,777,215 (FFFFFFh).

Table 8-8 RMV register selection code and bit width

Compatible mode	At writing		At reading	
	RCM3 ~ 0	RegWBF	RCM3 ~ 0	RegRBF
PCD46x1 mode	0000b	Bits 23 ~ 0	0000b	Bits 23 ~ 0
PCD45x1 compatible mode	∗000b	Bits 23 ~ 0	∗000b	Bits 23 ~ 0
PCD4500 compatible mode	∗000b	Bits 23 ~ 0	∗000b	Bits 23 ~ 0

∗: Don't Care

Table 8-9 RMV register access type per bit

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register operates as a down counter for positioning control.
It counts down by one every pulse output in any mode of continuous operation, origin return operation and positioning operation.
However, it does not count down in the case that count down operation control for positioning control is set to “stop counting”.
(When in PCD46x1 mode, RENV.DCSP = 1. In other cases, Register selection command.RCM3 = 1.)
The value of counter (number of remaining pulses) can be read both during operating and while stopped.
In positioning mode, start after setting number of output pulse to this register (counter).
After start, counter value decreases. When set number of pulses is output and the counter value becomes '0h', motor stops automatically.
In positioning mode, when writing a start command after setting '0h' to this register, pulses are not output and MSTS.BUSY and BSY output signal becomes stopping status soon.
At this time, INT signal is output when setting is “INT output is enabled at stopping”.

In positioning operation, even if operation is interrupted by a stop command and an external signal input, the remaining number of pulses is output by inputting a start command again because the counter value is the remaining number.

Because the counter value becomes '0h' after the set number of pulses output completes, you need to set the number to RMV register again even if the pulse number is the same as the previous time.

8-3-2. RFL

This is a 13-bit register to set a step value of FL speed.
Setting range is 1 (00001h) ~ 8,191 (1FFFh).

Table 8-10 RFL register selection code and bit width

Compatible mode	At writing		At reading	
	RCM3 ~ 0	RegWBF	RCM3 ~ 0	RegRBF
PCD46x1 mode	0001b	Bits 15 ~ 0	0001b	Bits 15 ~ 0
PCD45x1 compatible mode	∗001b	Bits 15 ~ 0	∗001b	Bits 15 ~ 0
PCD4500 compatible mode	∗001b	Bits 15 ~ 0	-	-

∗: Don't Care

Table 8-11 RFL register access type per bit

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

At high-speed start (with acceleration / deceleration), a motor starts at FL speed and accelerates to FH speed.
When writing a deceleration stop command in high-speed operation, a motor starts deceleration and stops when speed reaches to FL speed.
The relation between a setting value in RFL and FL speed varies according to “speed magnification” calculated by RMG setting value.

FL speed [pps] = (a setting value in RFL) × (speed magnification)

Note. If FL speed is set to 0, at stopping, output pulse of negative logic is locked to L level status and a motor may not in stop status. Set a value more than 1.

8-3-3. RFH

This is a 13-bit register to set step value of FH speed.
Setting range is 1 (0001h) ~ 8,191 (1FFFh).

Table 8-12 RFH register selection code and bit width

Compatible mode	At writing		At reading	
	RCM3 ~ 0	RegWBF	RCM3 ~ 0	RegRBF
PCD46x1 mode	0010b	Bits 15 ~ 0	0010b	Bits 15 ~ 0
PCD45x1 compatible mode	∗010b	Bits 15 ~ 0	∗010b	Bits 15 ~ 0
PCD4500 compatible mode	∗010b	Bits 15 ~ 0	-	-

∗: Don't Care

Table 8-13 RFH register access type per bit

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

At high-speed start (with acceleration / deceleration), a motor starts at FL speed and accelerates to FH speed.
The relation between a setting value in RFH and FH speed varies according to “speed magnification” calculated by a setting value in RMG.
FH speed [pps] = (a setting value in RFH) × (speed magnification)

Note. If FL speed is set to 0, at stopping, output pulse of negative logic is locked to L level status and a motor may not in stop status. Set a value more than 1.

8-3-4. RUD

This is a 16-bit register to set characteristics of acceleration and deceleration.
Setting range is 1 (0001h) ~ 65,535 (FFFFh).

Table 8-14 RUD register selection code and bit width

Compatible mode	At writing		At reading	
	RCM3 ~ 0	RegWBF	RCM3 ~ 0	RegRBF
PCD46x1 mode	0011b	Bits 15 ~ 0	0011b	Bits 15 ~ 0
PCD45x1 compatible mode	∗011b	Bits 15 ~ 0	∗011b	Bits 15 ~ 0
PCD4500 compatible mode	∗011b	Bits 15 ~ 0	-	-

∗: Don't Care

Table 8-15 RUD register and access type per bit

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The relation between a setting value in RUD and acceleration / deceleration time is as follows.

1. In linear acceleration / deceleration
   Acceleration / deceleration time [s] = (a setting value in RFH- a setting value in RFL) × (a setting value in RUD) / (reference clock frequency [Hz])

2. In S-curve acceleration / deceleration
   Acceleration / deceleration time [s] = (a setting value in RFH – a setting value in RFL) × (a setting value in RUD) × 2 / (reference clock frequency [Hz])

8-3-5. RMG

This is a 10-bit register to set speed magnification.
Setting range is 2 (0002h) ~ 1,023 (3FFh).

Table 8-16 RMG register selection code and bit width

Compatible mode	At writing		At reading	
	RCM3 ~ 0	RegWBF	RCM3 ~ 0	RegRBF
PCD46x1 mode	0100b	Bits 15 ~ 0	0100b	Bits 15 ~ 0
PCD45x1 compatible mode	∗100b	Bits 15 ~ 0	∗100b	Bits 15 ~ 0
PCD4500 compatible mode	∗100b	Bits 15 ~ 0	-	-

∗: Don't Care

Table 8-17 RMG register access type per bit

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The registers to set speed (RFL and RFH) can set speed step value 1 ~ 8,191. This register is use to set the relation between speed step value and output pulse speed.
Output pulse speed [pps] = (a value in the register to set speed) × (speed magnification)
Speed magnification [times] = (reference clock frequency [Hz]) / (a setting value in RMG × 8,192)

Table 8-18 A setting value in RMG and magnification (Typical example)

RMG set value	Magnification
600 (258h)	1 times
300 (12Ch)	2 times
120 (078H)	5 times

RMG set value	Magnification
60 (03Ch)	10 times
30 (01Eh)	20 times
12 (00Ch)	50 times

RMG set value	Magnification
6 (006h)	100 times
3 (003h)	200 times
2 (002h)	300 times

8-3-6. RDP

This is a 24-bit register to set a ramping-down point.

Setting range changes according to setting method of a ramping-down point.

Table 8-19 RDP register selection code and bit width

Compatible mode	At writing		At reading	
	RCM3 ~ 0	RegWBF	RCM3 ~ 0	RegRBF
PCD46x1 mode	0101b	Bits 23 ~ 0	0101b	Bits 23 ~ 0
PCD45x1 compatible mode	∗101b	Bits 23 ~ 0	∗101b	Bits 15 ~ 0
PCD4500 compatible mode	∗101b	Bits 23 ~ 0	-	-

∗: Don't Care

Table 8-20 RDP register access type per bit

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

In PCD45x1 compatible mode: bits 23 ~ 16 are for write only. (Read is not available.)

This register is used to set the timing to start deceleration in positioning operation mode.

The setting value in this register is disabled in other than positioning operation mode (Control mode command.CCM2=0).

There are two setting methods of a ramping-down point: manual setting and automatic setting. This is selected by RENV.ASDP.

The definition of setting value in this register varies according to the method to set a ramping-down point.

1. Manual setting (RENV.ASDP = 0)

   Set timing to start deceleration by a number of remaining pulses.

   Setting range is 0 ~ 16,777,215 (FFFFFFh).

   When RPLS (number of remaining pulses) ≤ (a setting value in RDP), deceleration starts.

2. Automatic setting (RENV.ASDP = 1)

   Set a correction value with a sign for an automatic setting value.

   When a positive number is set, a motor starts decelerations earlier. After deceleration is complete, a motor operates at FL speed and stops.

   When negative number is set, a motor starts deceleration later. Before the speed reaches FL speed, the motor stops.

   The automatic setting value is “0” at the start and increases by counting pulses output during acceleration.

   If you want to use an automatic setting value, set to “0” (000000h).

   The setting range of a correction amount is -8,388,608 (800000h) ~ +8,388,607 (7FFFFFh).

   When RPLS (number of remaining pulses) ≤ (automatic setting value) + (a setting value in RDP), deceleration starts.

   Automatic setting value is “0” at the start and increases by counting pulses output during acceleration.

   It decreases by counting pulses output during deceleration.

   In both manual setting and automatic setting, if the above condition to start deceleration is met at the start, a motor operates at the FL speed without acceleration.

8-3-7. RIDL

This is a 3-bit register to set number of idling pulses

Setting range is 0(0h) ~ 7 (7h).

Table 8-21 RIDL register selection code and bit width

Compatible mode	At writing		At reading	
	RCM3 ~ 0	RegWBF	RCM3 ~ 0	RegRBF
PCD46x1 mode	0110b	Bits 7 ~ 0	0110b	Bits 7 ~ 0
PCD45x1 compatible mode	∗110b	Bits 7 ~ 0	∗110b	Bits 7 ~ 0
PCD4500 compatible mode	∗110b	Bits 7 ~ 0	-	-

∗: Don't Care

Table 8-22 RIDL register access type per bit

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	R/W	R/W	R/W

Motor starts acceleration after the LSI outputs a number of pulses set in this register in high-speed (with acceleration / deceleration) start.

When “0” is set in this register, the motor starts acceleration at the start. Therefore, the initial pulse cycle is shorter than the cycle of FL speed.

About the detail of idling pulse output, see 11-2 Idling pulse output.

8-3-8. RENV

This is a 24-bit register to set operation environment. 16 bits (bits 15~0) are used actually and upper data (bits 23~16) is for shipping inspection. Make sure to set '00h'.

Table 8-23 RENV register selection code and bit width

Compatible mode	At writing		At reading	
	RCM3 ~ 0	RegWBF	RCM3 ~ 0	RegRBF
PCD46x1 mode	0111b	Bits 23 ~ 0	0110b	Bits 15 ~ 0
PCD45x1 compatible mode	∗111b	Bits 23 ~ 0	∗101b	Bits 23 ~ 16
PCD4500 compatible mode	∗111b	Bits 23 ~ 0	-	-

∗: Don't Care

Table 8-24 RENV register access type per bit

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W	W	W	W	W	W	W	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

In PCD45x1 compatible mode: bits 15 ~ 8 are for write only (Read is not available.)

Table 8-25 Bit names of RENV register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IPM4	IPM3	IPM2	IPM1	IOPM	MSKM	PREV	PSTP	ORRS	ORDS	ELDS	SPDS	ASDP	DCSP	46MD	PMD

Table 8-26 Description of RENV register

Bit	Bit name	Description
0	PMD	Select output pulse mode from +PO/PLS and -PO/DIR terminals. (See 11-5. Output pulse mode) 0: Two pulse mode (+PO,-PO) [+] direction pulse from +PO terminal and[-] direction pulse from –PO terminal 1: Common pulse mode (PLS, DIR) Output pulse from PLS terminal and direction signal output from DIR terminal. (H = [+] direction, L = [-] direction)
1	46MD	Compatible mode selection ∗1 0: PCD45x1 compatible mode 1: PCD46x1 mode However, with serial I/F, it is fixed to '1' (Even if '0' is written, it is ignored.)
2	DCSP	Control the down counter for positioning. (available in PCD46x1 mode only) 0: Count down every output pulse 1: Stop counting When RENV.46MD = 0, the down counter for positioning is controlled by the setting of Register selection command.RCM3.
3	ASPD	Select the setting of a ramping-down point 0: Manual setting 1: Auto setting
4	SPDS	Select stop method by STP input 0: Stop immediately 1: Decelerate and stop
5	ELDS	Select stop method by +EL and –EL input. 0: Stop immediately 1: Decelerate and stop
6	ORDS	Select stop method by ORG input 0: Stop immediately 1: Decelerate and stop
7	ORRS	Set automatic reset of RCUN (current position counter) 0: Auto reset OFF 1: Reset at L level of ORG input in origin return operation ∗2
8	PSTP	Select count operation of RCUN (Current position counter) 0: Count every pulse output (Also count when Output mode command.OCM1 = 1) 1: Stop counting
9	PREV	Select count direction of RCUN (Current position counter) 0: Count forward in (+) direction operation and count backward in (-) direction operation. 1: Count backward in (+) direction operation and count forward in (-) direction operation.
10	MSKM	Output setting when excitation sequence output is masked. (When Output mode command.OCM2 = 1) 0: PH1 = L, PH2 = L, PH3 = L, PH4 = L 1: PH1 = L, PH2 = L, PH3 = H, PH4 = H
11	IOPM	Select functions of PH1 / P1 ~ PH4 / P4 terminal ∗3 0: Use as PH1 ~ PH4 (Excitation sequence output) output terminals. 1: Use as P1 ~ P4 (general-purpose port) input / output terminals.
12	IPM1	Select specifications of P1 general-purpose input / output terminal ∗4 0: General-purpose output terminal 1: General-purpose input terminal
13	IPM2	Select specifications of P2 general-purpose input / output terminal ∗4 0: General-purpose output terminal 1: General-purpose input terminal
14	IPM3	Select specifications of P3 general-purpose input / output terminal ∗4 0: General-purpose output terminal 1: General-purpose input terminal
15	IPM4	Select specifications of P4 general-purpose input / output terminal ∗4 0: General-purpose output terminal 1: General-purpose input terminal

∗1: Before set RENV.46MD to "1", set Output mode command.OCM5 to "1" in advance.

∗2: Pulse cycle completes at falling edge of ORG signal while pulses are not output and at L level of ORG signal while pulses are output.

∗3: When RENV.IOPM = 0, setting of RENV.IPM1 ~ IPM4 is disabled.

∗4: In default status, they are output terminals of PH1 ~ PH4. If they are used as general-purpose input terminals, See “14-1-6 When general-purpose input / output ports (P1 ~ P4) are used as general-purpose input”

8-3-9. RCUN

This is a 24-bit current position counter.

Setting range is 0 (000000h) ~ 16,777,215 (FFFFFFh) or -8,388,608 (800000h) ~ +8,388,607 (7FFFFFh) and varies according to number control of control software.

Table 8-27 RCUN register selection code and bit width

Compatible mode	At writing		At reading	
	RCM3 ~ 0	RegWBF	RCM3 ~ 0	RegRBF
PCD46x1 mode	1000b	Bits 23 ~ 0	1000b	Bits 23 ~ 0
PCD45x1 compatible mode	-	-	-	-
PCD4500 compatible mode	-	-	-	-

Table 8-28 RCUN register access type per bit

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This value becomes FFFFFFh after counting backward from 000000h and becomes 000000h after counting forward from FFFFFh.

The register counts every pulse output when RENV.PSTP=0, and does not count when RENV.PSTP=1 though pulses are outputs.

This register count forward in (+) direction operation and count backward in (-) direction operation with RENV.PREV=0. With RENV.PREV=1, the count direction is reverse.

With RENV.ORRS=1 in origin return operation, this counter is reset automatically at origin point. For detail, see “9-2. Origin return mode”.

8-3-10. RSTS

This is a 16-bit register to monitor extended status.

Table 8-29 RSTSregister selection code and bit width

	At writing		At reading	
	RCM3 ~ 0	RegWBF	RCM3 ~ 0	RegRBF
PCD46x1 mode	-	-	1001b	Bits 15 ~ 0
PCD45x1 compatible mode	-	-	∗111b	Bits 15 ~ 0
PCD4500 compatible mode	-	-	∗001~ ∗111b	Bits 7 ~ 0

∗: Don't Care

Table 8-30 RSTS register access type per bit

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

In PCD4500 compatible mode: bits 15 ~ 8 are for read only.

Table 8-31 RSTS register bit name

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SINT	SOTS	SPPO	SMPO	SPH4	SPH3	SPH2	SPH1	SPHZ	SPSD	SMSD	SSTA	SSTP	SORG	SPEL	SMEL

For the detail of extended status, see ”7-2. Extended status”.

8-3-11. RIDC

This is an 8-bit register and Product information code.

Table 8-32 RIDC register selection code and bit width

mode	At writing		At reading	
	RCM3 ~ 0	RegWBF	RCM3 ~ 0	RegRBF
PCD46x1 mode	-	-	0111b	Bits 23 ~ 16
PCD45x1 compatible mode	-	-	∗111b	Bits 23 ~ 16
PCD4500 compatible mode	-	-	-	-

∗: Don't Care

Table 8-33 RIDC register access type per bit

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	R	R	R	R	R	0	0	R

Table 8-34 Bit names of RIDC register

7	6	5	4	3	2	1	0
IDC3	IDC2	IDC1	IDC0	VRC	0	0	S46M

For product information code in detail, refer to ”7-3. Product information code”

8-3-12. RIOP

This is a 6 bit register to set and monitor general-purpose input / output port (PH1 / P1 ~ PH4 / P4) that can be used as excitation sequence output.

Table 8-35 RIOP register selection code and bit width

Compatible mode	At writing		At reading	
	RCM3 ~ 0	RegWBF	RCM3 ~ 0	RegRBF
PCD46x1 mode	1010b	Bits 7 ~ 0	1010b	Bits 7 ~ 0
PCD45x1 compatible mode	-	-	-	-
PCD4500 compatible mode	-	-	-	-

Table 8-36 RIOP register access type

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	R	R	W/R	W/R	W/R	W/R

Table 8-37 RIOP Register bit name

7	6	5	4	3	2	1	0
0	0	MFH	MUB	CP4	CP3	CP2	CP1

Table 8-38 Description of RIOP register

Bit	Bit name	Description
0	CP1	P1 terminal control (at writing) PH1 / P1 terminal status monitor (at reading) 0: L level 1: H level
1	CP2	P2 terminal control (at writing) PH2 / P2 terminal status monitor (at reading) 0: L level 1: H level
2	CP3	P3 terminal control (at writing PH3 / P3 terminal status monitor (at reading) 0: L level 1: H level
3	CP4	P4 terminal control (at writing) PH4 / P4 terminal status monitor (at reading) 0: L level 1: H level
4	MUB	U/B terminal status monitor (writing is disabled) 0: L level 1: H level
5	MFH	F/H terminal status monitor (writing is disabled) 0: L level 1: H level
7~6	Undefined	(Always '00b')

By writing to this register, output level of general-purpose output ports is set.

By reading this register, status of general-purpose input / output ports is monitored.

8-3-13. RSPD

This is read-only current speed monitor and a 16 bit register.

The unit is the same speed step value as RFL and RFH register values.

The setting range is (0000h) ~ 8,191 (FFFFh).

Table 8-39 RSPD register selection code and bit width

Compatible mode	At writing		At reading	
	RCM3 ~ 0	RegWBF	RCM3 ~ 0	RegRBF
PCD46x1 mode	-	-	0110b	Bits 23 ~ 8
PCD45x1 compatible mode	-	-	∗110b	Bits 23 ~ 16
PCD4500 compatible mode	-	-	-	-

∗: Don't Care

Table 8-40 RSPD register bit unit and access type

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RSPD monitor value is 0 while stopping.

The relation between RSPD monitor value and operation speed varies according to speed magnification calculated by RMG setting value.

Operation speed [pps] = (RSPD monitor value) × (speed magnification)

8-3-14. RSPO

This is a 6-bit register to monitor output setting of common ports (SP0 ~ SP5)

This register is available with serial I/F only.

There is one RSPO register per LSI. Axis selection is ignored.

With parallel I/F, write is disabled and read value is '00h'.

Table 8-41 RSPO register selection code and bit width

Compatible mode	At writing		At reading	
	RCM3 ~ 0	RegWBF	RCM3 ~ 0	RegRBF
PCD46x1 mode	1011b	bits 7 ~ 0	1011b	bits 7 ~ 0
PCD45x1 compatible mode	-	-	-	-
PCD4500 compatible mode	-	-	-	-

Table 8-42 RSPO register access type per bit

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	W/R	W/R	W/R	W/R	W/R	W/R

Table 8-43 RSPO register bit name

7	6	5	4	3	2	1	0
0	0	SPO5	SPO4	SPO3	SPO2	SPO1	SPO0

Table 8-44 Description of RSPO register

Bit	Bit name	Description
0	SPO0	SP0 terminal control (at writing) / SP0 terminal status monitor (at reading) 0: L level 1: H level
1	SPO1	SP1 terminal control (at writing / SP1 terminal status monitor (at reading) 0: L level 1: H level
2	SPO2	SP2 terminal control (at writing) / SP2 terminal status monitor (at reading) 0: L level 1: H level
3	SPO3	SP3 terminal control (at writing) / SP3 terminal status monitor (at reading) 0: L level 1: H level
4	SPO4	SP4 terminal control (at writing) / SP4 terminal status monitor (at reading) 0: L level 1: H level
5	SPO5	SP5 terminal control (at writing) / SP5 terminal status monitor (at reading) 0: L level 1: H level
7~6	Not defined	(Always '00b')

8-3-15. RSPM

This is a 6-bit register to set input and output for common ports (SP0 ~ SP5).

this register is available with serial I/F only.

There is one RSPM register per LSI. Axis selection is ignored.

With parallel I/F, write is disabled and read value is '00h'.

Table 8-45 RSPM register selection code and bit width

Compatible mode	When writing		When reading	
	RCM3 ~ 0	RegWBF	RCM3 ~ 0	RegRBF
PCD46x1 mode	1100b	Bits 7 ~ 0	1100b	bits 7 ~ 0
PCD45x1 compatible mode	-	-	-	-
PCD4500 compatible mode	-	-	-	-

Table 8-46 RSPM register access type per bit

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	W/R	W/R	W/R	W/R	W/R	W/R

Table 8-47 Bit name of RSPM register

7	6	5	4	3	2	1	0
0	0	SPM5	SPM4	SPM3	SPM2	SPM1	SPM0

Table 8-48 Description of RSPM register

Bit	Bit name	Description
0	SPM0	Select specifications of SP0 general-purpose input / output terminal 0: General-purpose output terminal 1: General-purpose input terminal
1	SPM1	Select specifications of SP1 general-purpose input / output terminal 0: General-purpose output terminal 1: General-purpose input terminal
2	SPM2	Select specifications of SP2 general-purpose input / output terminal 0: General-purpose output terminal 1: General-purpose input terminal
3	SPM3	Select specifications of SP3 general-purpose input / output terminal 0: General-purpose output terminal 1: General-purpose input terminal
4	SPM4	Select specifications of SP4 general-purpose input / output terminal 0: General-purpose output terminal 1: General-purpose input terminal
5	SPM5	Select specifications of SP5 general-purpose input / output terminal 0: General-purpose output terminal 1: General-purpose input terminal
7~6	Undefined	(Always '00b')

9. Operation modes

Note.
Operation procedure may vary according to compatible modes (PCD46x1 mode, PCD45x1 compatible mode and PCD4500 compatible mode). The followings explain PCD46x1 mode.

There are four modes in operation modes.

- Continuous mode
- Positioning mode
- Origin return mode
- Timer mode

Operation mode is selected by setting control mode command, output mode command and RENV register.

Table 9-1 Operation mode selection

Output mode command	Control mode command		RENV register	Operation mode
OCM1	CCM2	CCM0	PSTP	
0	0	0	0	Continuous mode
0	0	1	0	Origin return mode
0	1	1	0	Origin return mode (Maximum feed amount control)
0	1	0	0	Positioning mode
1	1	0	1	Timer mode

9-1. Continuous operation mode

This is a mode to continue operation until a stop command is written after operation starts by inputting a start command.

The direction of operation is set by Control mode command.CCM3. (0:[+] direction, 1:[-] direction)

RMV Read value (down counter value for positioning control) decreases from the value at the start.

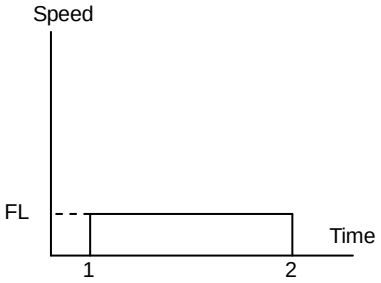
Table 9-2 Setting items for continuous mode

Operation direction in continuous mode <CCM3> 0: [+] direction 1: [-] direction	Control mode command (WRITE) 7 0 0 1 - - n 0 - 0
Pulse output control <OCM1> 0: Output pulses 1: Does not output pulses	Output mode command (WRITE) 7 0 1 1 1 - - - n -
Set count operation of RCUN (current position counter) <RENV.PSTP> 0: Count pulse output (Count even when Output mode command.OCM1=1) 1: Stop counting	RENV register (WRITE) 15 8 - - - - - - - n

9-1-1. Procedure example of [+] direction FL constant speed continuous operation

1. At the start

COMBF ← 40h (Control mode command: [+] direction)
COMBF ← E0h (Output mode command: extended monitor, pulses are output.)
COMBF ← 87h (Register selection command: RENV)
RegWBF upper data (bits 23~16) ← 00h
RegWBF middle data (bits 15~ 8) ← 00h
RegWBF lower data (bits 7~ 0) ← 02h (PCD46x1 mode)
COMBF ← 81h (Register selection command: RFL 000100h)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits15~ 8) ← 01h
RegWBF lower data (bits 7~ 0) ← 00h
COMBF ← 84h (Register selection command: RMG 000258h)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits 15~ 8) ← 02h
RegWBF lower data (bits 7~ 0) ← 58h
COMBF ← 10h (Start mode command: FL constant speed start)



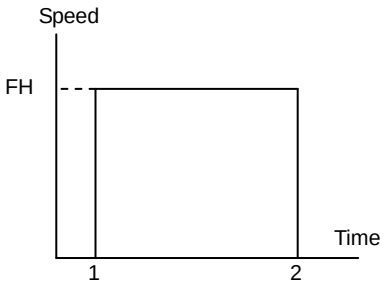
2. At the stop

COMBF ← 08h (Start mode command: stop immediately)

9-1-2. Procedure example of [-] direction FH constant speed continuous operation

1. At the start

COMBF ← 48h (Control mode command: [-] direction)
COMBF ← E0h (Output mode command: Extended monitor, pulses are output.)
COMBF ← 87h (Register selection command: RENV)
RegWBF upper data (bits 23~16) ← 00h
RegWBF middle data (bits 5~ 8) ← 00h
RegWBF lower data (bits 7~ 0) ← 02h (PCD46x1 mode)
COMBF ← 82h (Register selection command: RFH 001000h)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits 15~ 8) ← 10h
RegWBF Lower data (bits 7~ 0) ← 00h
COMBF ← 84h (Register selection command: RMG 000258h)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits 15~ 8) ← 02h
RegWBF lower data (bits 7~ 0) ← 58h
COMBF ← 11h (Start mode command: FH constant speed start)



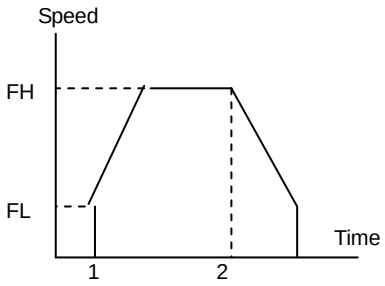
2. At the stop

COMBF ← 08h (Start mode command: immediately stop)

9-1-3. Procedure example of [+] direction FH high-speed continuous operation

1. At the start

COMBF ← 40h (Control mode command: [+] direction)
COMBF ← E0h (Output mode command: Extended monitor, pulses are output.)
COMBF ← 87h (Register selection command: RENV)
RegWBF upper data (bits 23~16) ← 00h
RegWBF middle data (bits 15~ 8) ← 00h
RegWBF lower data (bits 7~ 0) ← 02h (PCD46x1 mode)
COMBF ← 81h (register selection command: RFL 000100h)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits 15~ 8) ← 01h
RegWBF lower data (bits 7~ 0) ← 00h
COMBF ← 82h (Register selection command: RFH 001000h)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits 15~ 8) ← 10h
RegWBF lower data (bits 7~ 0) ← 00h
COMBF ← 83h (register selection command: RUD 001000h)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits 15~ 8) ← 10h
RegWBF lower data (bits 7~ 0) ← 00h
COMBF ← 84h (register selection command: RMG 000258h)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits 15~ 8) ← 02h
RegWBF lower data (bits 7~ 0) ← 58h
COMBF ← 15h (Start mode command: FH high speed start)



2. At the stop

COMBF ← 1Dh (Start mode command: Deceleration and stop)

9-2. Origin return mode

After the start, a motor operates until an origin signal (ORG) turns ON (L level).
Operation direction is set by Control mode command.CCM3. (0: [+] direction, 1: [-] direction)
Even when a start command is written with ORG terminal ON (L level), a motor does not start. However, when an INT signal is set to be output when a motor stops, an INT signal is output.
You can control the maximum feed amount using positioning control with Control mode command.CCM2=1. In this case, you can set the maximum feed amount in the RMV to prevent from endless operation that caused by breakage of origin switch.
At the FH high-speed start, input an SD signal and decelerate operation to FL speed and stop by an ORG signal. With RENV.ORRS=1, RCUN (current position counter) is reset automatically at the falling edge of ORG signal input.
With RENV.ORRS=1 and RENV.ORDS=1, RCUN (current position counter) is reset when ORG input turns ON (L level) and operation starts deceleration. After the speed reaches to FL speed, a motor stops. The stop position is not the origin point. However, the difference from the origin point can be controlled by a value in RCUN. (SD sensor can be omitted.)
Read value in RMV (Down counter value for positioning control) decreases from the value at the start.

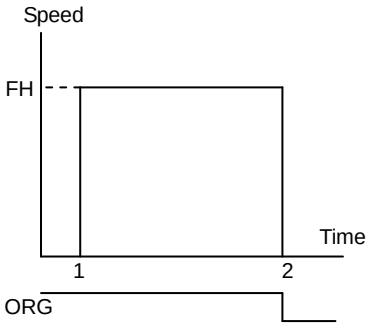
Table 9-3 Setting items for origin return mode

Operation direction in origin return mode <CCM3> 0: [+] direction 1: [-] direction	Control mode command (WRITE) 7 0 0 1 - - n 0 - 1
Operation direction in origin return mode with maximum feed amount control <CCM3> 0: [+] direction 1: [-] direction	Control mode command (WRITE) 7 0 0 1 - - n 1 - 1
SD signal control <CCM1> 0: +SD or -SD input are disabled 1: Deceleration to FL speed by turning +SD or -SD ON.	Control mode command (WRITE) 7 0 0 1 - - - - n 1
Pulse output control <OCM2> 0: Outputs pulses. 1: Does not output pulses	Output mode command (WRITE) 7 0 1 1 - - - - n -
Stop method by ORG input <RENV.ORDS> 0: Stop immediately when ORG input turns ON 1: Decelerate and stop when ORG input turns ON.	RENV register (WRITE) 7 0 - n - - - - - -
RCUN automatic reset by inputting ORG <RENV.ORRS> 0: RCUN automatic reset OFF 1: RCUN is reset automatically at the falling edge of ORG input.	RENV register (WRITE) 7 0 n - - - - - - -
Set the count operation of RCUN (Current position counter) <RENV.PSTP> 0: Count every pulse output (Count even when Output mode command.OCM1=1) 1: Stop counting	RENV register (WRITE) 15 8 - - - - - - - n

9-2-1. Procedure example of [+] direction of FH constant speed origin return operation

1. At the start

COMBF ← 41h (Control mode command: origin return mode, [+] direction)
COMBF ← E0h (Output mode command: Extended monitor, pulses are output.)
COMBF ← 87h (Register selection command: RENV)
RegWBF upper data (bits 23~16) ← 00h
RegWBF middle data (bits 15~ 8) ← 00h
RegWBF lower data (bits 7~ 0) ← 02h (PCD46x1 mode)
COMBF ← 82h (Register selection command: RFH 001000h)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits 15~ 8) ← 10h
RegWBF lower data (bits 7~ 0) ← 00h
COMBF ← 84h (Register selection command: RMG 000258h)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits 15~ 8) ← 02h
RegWBF lower data (bits 7~ 0) ← 58h
COMBF ← 11h (Start mode command: FH constant speed start)



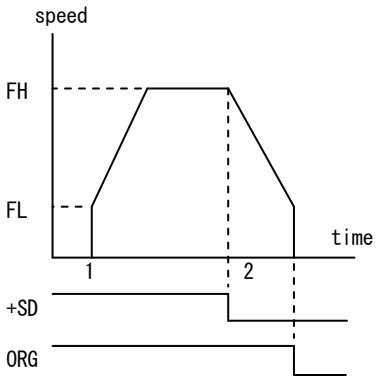
2. At the stop

A motor stops automatically by turning an ORG signal input ON (L level).

9-2-2. Procedure example of [+] direction of FH high speed origin return operation

1. At the start

COMBF ← 43h (Control mode command: origin return mode and SD are enabled, [+] direction)
COMBF ← E0h (Output mode command: extended monitor, pulse are output.)
COMBF ← 87h (Register selection command: RENV)
RegWBF upper data (bits 23~16) ← 00h
RegWBF middle data (bits 15~ 8) ← 00h
RegWBF lower data (bits 7~ 0) ← 02h (PCD46x1 mode)
COMBF ← 81h (Register selection command: RFL 000100h)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits 15~ 8) ← 01h
RegWBF lower data (bits 7~ 0) ← 00h
COMBF ← 82h (Register selection command: RFH 001000h)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits 15~ 8) ← 10h
RegWBF lower data (bits 7~ 0) ← 00h
COMBF ← 83h (Register selection command: RUD 001000h)
RegWBF upper data (bit 23~16) ← 00h (can be omitted)
RegWBF middle data (bit 15~ 8) ← 10h
RegWBF lower data (bit 7~ 0) ← 00h
COMBF ← 84h (Register selection command: RMG 000258h)
RegWBF upper data (bit 23~16) ← 00h (can be omitted)
RegWBF middle data (bit 15~ 8) ← 02h
RegWBF lower data (bit 7~ 0) ← 58h
COMBF ← 15h (Start mode command: FH high speed start)



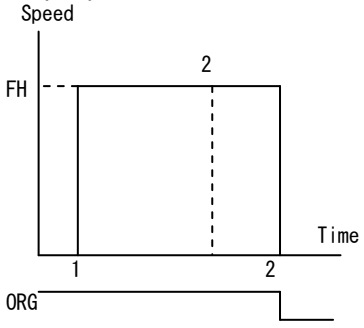
2. At the stop

A motor decelerates when SD input turns ON (L level) and stops automatically when ORG signal input turns ON (L level).

9-2-3. Procedure example of [+] direction FH constant speed origin return operation with maximum feeding amount control.

1. At the start

COMBF ← 45h (Control mode command: Origin return mode (with maximum feeding amount control), [+] direction)
COMBF ← E0h (Output mode command: extended monitor, pulses are output.)
COMBF ← 87h (Register selection command: RENV)
RegWBF upper data (bits 23~16) ← 00h
RegWBF middle data (bits 15~ 8) ← 00h
RegWBF lower data (bits 7~ 0) ← 02h (PCD46x1 mode)
COMBF ← 80h (Register selection command: RMV 004E20h)
RegWBF upper data (bits 23~16) ← 00h
RegWBF middle data (bits 15~ 8) ← 4Eh
RegWBF lower data (bits 7~ 0) ← 20h
COMBF ← 82h (Register selection command: RFH 1000h)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits 15~ 8) ← 10h
RegWBF lower data (bits 7~ 0) ← 00h



COMBF ← 84h (Register selection command: RMG 0258h)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits 15~ 8) ← 02h
RegWBF lower data (bits 7~ 0) ← 58h
COMBF ← 11h (Start mode command: FH constant speed start)

2. A motor stop automatically by turning ORG signal (L level) or outputting a setting pulse number of pulses (RMV) are output.

9-3. Positioning mode

This is a mode to operate positioning specified by pulse number and direction.
The operation direction is set by Control mode command.CCM3.

If output pulse number is set in RMV register and operation starts, a value in RMV decreases per pulse output. When the value reaches to 0, the motor stops.

The RMV setting value becomes 0 when positioning operation is complete. Set a value every time even if the value you want to set is the same as the previous setting.
With a setting value in RMV = 0, a motor does not start even if a start command is written. However, when INT signal is set to be output when a motor stops, INT signal is output.

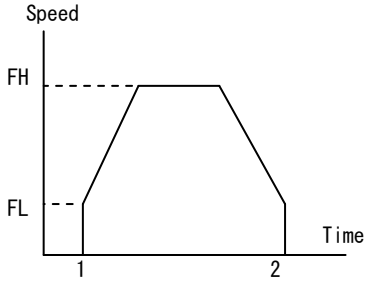
Table 9-4 Setting items of positioning mode

Operation direction in positioning mode <CCM3> 0: [+] direction 1: [-] direction	Control mode command (WRITE) 7 0 0 1 - - n 1 - -
SD signal control <CCM1> 0: SD input signal is disabled 1: Decelerates to FL speed by inputting SD signal ON.	Control mode command (WRITE) 7 0 0 1 - - - 1 n -
Pulse output control <OCM2> 0: Outputs 1: Does not output	Output mode command (WRITE) 7 0 1 1 - - - - n -
Set the count operation of RCUN (current position counter) <RENV.PSTP> 0: Count every pulse output (Count even when output mode command.OCM1=1) 1: Stop counting	RENV register (WRITE) 15 8 - - - - - - - n

9-3-1. Procedure example of [+] direction 1000 pulse FH high speed positioning operation

1. At the start

COMBF ← 44h (Control mode command: positioning mode, [+] direction)
COMBF ← E0h (Output mode command: extended monitor, pulses are output.)
COMBF ← 87h (Register selection command: RENV)
RegWBF upper data (bits 23~16) ← 00h
RegWBF middle data (bits 15~ 8) ← 00h
RegWBF lower data (bits 7~ 0) ← 0Ah (ramping-down point auto setting, PCD46x1 mode)
COMBF ← 80h (Register selection command: RMV 0003E8h = 1000 pulse)
RegWBF upper data (bits 23~16) ← 00h
RegWBF middle data (bits 15~ 8) ← 03h
RegWBF lower data (bits 7~ 0) ← E8h
COMBF ← 81h (Register selection command: RFL 000100h)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits 15~ 8) ← 01h
RegWBF lower data (bits 7~ 0) ← 00h
COMBF ← 82h (Register selection command: RFH 001000h)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits 15~ 8) ← 10h
RegWBF lower data (bits 7~ 0) ← 00h
COMBF ← 83h (Register selection command: RUD 001000h)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits 15~ 8) ← 10h
RegWBF lower data (bits 7~ 0) ← 00h
COMBF ← 84h (Register selection command: RMG 000258h)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits 15~ 8) ← 02h
RegWBF lower data (bits 7~ 0) ← 58h
COMBF ← 15h (Start mode command: FH high speed start)



2. At the stop

The motor stops automatically at the position of 1000 pulse.

9-4. Timer mode

This is a mode to use operation time as a timer while masking pulse output (Output mode command.OCM1 =1) in positioning operation.

(Setting time) = (Pulse cycle of setting speed) x (number of setting pulses)

In timer mode, a motor stops when an STP signal becomes ON (L level) or a stop command is written. The motor does not stop even when the EL signal or ORG signal are ignored.

9-4-1. Procedure example to use this mode as a 100 [msec] timer

The time to output 100 pulses at 1000 pps is 100 msec. Therefore, after you set the speed to "1000 pps", do the followings. INT output is used to determine stopping.

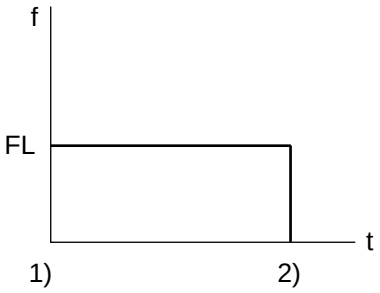
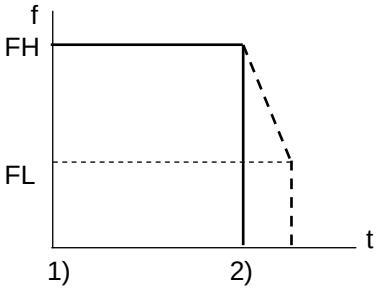
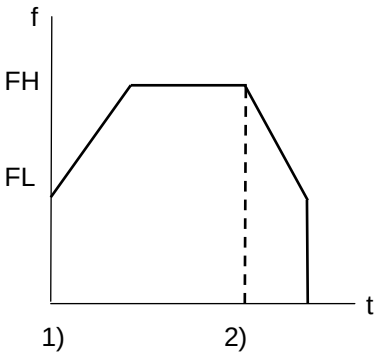
COMBF ← 44h (Control mode command: positioning mode, [+] direction)
COMBF ← E2h (Output mode command: extended monitor, pulse output is masked)
COMBF ← 87h (Register selection command: RENV)
RegWBF upper data (bits 23~16) ← 00h
RegWBF middle data (bits 15~ 8) ← 00h
RegWBF lower data (bits 7~ 0) ← 02h (PCD46x1 mode)
COMBF ← 80h (Register selection command: RMV 000064h = 100 pulses)
RegWBF upper data (bits 23~16) ← 00h
RegWBF middle data (bits 15~ 8) ← 00h
RegWBF lower data (bits 7~ 0) ← 64h
COMBF ← 81h (Register selection command: RFL 0003E8h = 1000)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits 15~ 8) ← 03h
RegWBF lower data (bits 7~ 0) ← E8h
COMBF ← 84h (Register selection command: RMG 000258h 1x)
RegWBF upper data (bits 23~16) ← 00h (can be omitted)
RegWBF middle data (bits 15~ 8) ← 02h
RegWBF lower data (bits 7~ 0) ← 58h
COMBF ← 30h (Start mode command: FL constant speed start, INT is output at stopping)

If an interrupt occurs, time (100 msec) is up.

10. Speed pattern

10-1. Speed pattern

Table 10-1 Speed pattern

Speed pattern	Continuous mode	Positioning mode
FL constant speed operation  	1) Write FL constant speed start (10h) command 2) Stop by writing immediate stop (08h) / deceleration and stop command (1Dh)	1) Write FL constant speed start (10h) command 2) Stop by positioning counter = 0 or writing immediate stop (08h) / deceleration stop (1Dh) command
FH constant speed operation  	1) Write FH constant speed start (11h) command 2) Stop by writing immediate stop (08h) command	1) Write FH constant speed start (11h) command 2) Stop by positioning counter = 0 or immediate stop (08h) command
	Decelerates and stops when deceleration and stop command (1Dh) is written in the case of 2).	
FH high speed operation  	1) Write FH high speed start (15h) command 2) Start deceleration by writing deceleration stop command (1Dh).	1) Write FH high speed start (15h) command 2) Start deceleration when a ramping-down point is reached or by writing a deceleration stop (1Dh) command ∗ Motor stops immediately when the ramping-down point setting is set to manual (RENV.ASDP = 0) and a ramping-down setting value (RDP)=0.

10-2. Speed pattern settings

Specify the speed pattern using the registers shown in the table below.

If the register setting to be set is the same as the previous value, there is no need to write to the register again. However, because RMV values counts downward in operation even if you want to repeat same feed amount for positioning operation, please write the feed amount to the RMV register every time,

Table 10-2 Setting items of speed pattern

Register	Description	Bit width	Setting range
RMV	Set feed amount	24	0 ~ 16,777,215 (FFFFFFh)
RFL	Set FL speed	13	1 ~ 8,191 (1FFFh)
RFH	Set FH speed	13	1 ~ 8,191 (1FFFh)
RUD	Set acceleration / deceleration rate	16	1 ~ 65,535 (FFFFh)
RMG	Set magnification	10	2 ~ 1,023 (3FFh)
RDP	Set ramping-down point	24	0 ~ 16,777,215 (FFFFFFh)
RDIL	Set idling pulse	3	0 ~ 7 (7h)

[The places where register data are used in acceleration / deceleration operation]

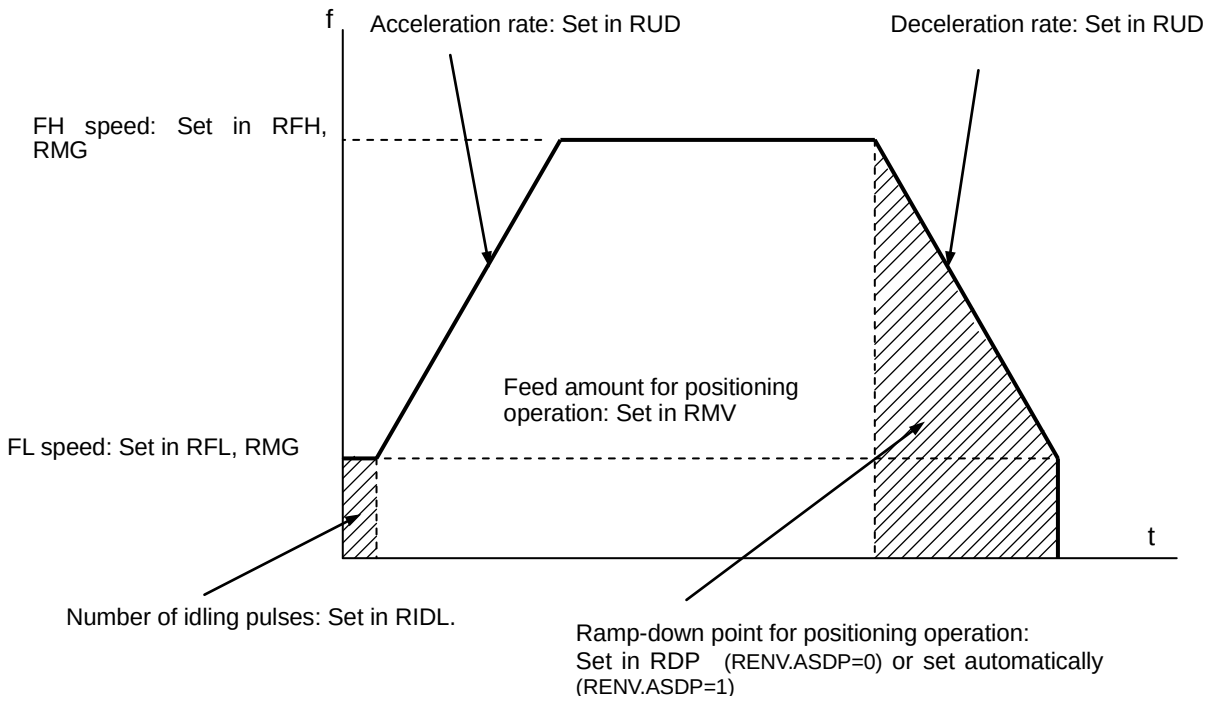


Figure 10-1 Outline of speed pattern setting

◆ RFL: FL speed setting register (13-bit)

Specify initial speed at FL constant speed and high-speed operation (acceleration / deceleration operation) in the range of 1 (0001h) ~ 8,191 (1FFFh). The speed [pps] is a product of multiplying magnification rate by the a setting value in RMG.

FL speed [pps] = RFL x magnification rate

◆ RFH: FH speed setting register (13-bit)

Specify operation speed at FH constant speed and high-speed operation (acceleration / deceleration operation) in the range of 1 (0001h) ~ 8,191 (1FFFh). In high-speed operation (acceleration / deceleration operation), specify a value larger than a setting value in RFL. The speed [pps] is a product of multiplying magnification rate by a setting value in RMG.

FH speed [pps] = RFH x magnification rate

◆ RUD: Acceleration / deceleration rate setting register (16-bit)

Specify the acceleration / deceleration characteristics when high-speed operation (acceleration / deceleration operation) is set in the range of 1 (0001h) ~ 65,535 (FFFFh).

Relationship between the value entered and the acceleration / deceleration time will be as follows:

1. Linear acceleration / deceleration (Control mode command.CCM5=0)

$$\text{Acceleration / deceleration time [sec]} = \frac{(\text{RFH} - \text{RFL}) \times \text{RUD}}{\text{Reference clock frequency [Hz]}}$$

2. S-curve acceleration / deceleration (Control mode command.CCM5=1)

$$\text{Acceleration / deceleration time [sec]} = \frac{(\text{RFH} - \text{RFL}) \times \text{RUD} \times 2}{\text{Reference clock frequency [Hz]}}$$

◆ RMG: Speed magnification rate register (10-bit)

Specify the relationship between setting values in RFL and RFH and the speed in the range of 2 (002h) ~ 1,023 (3FFh).

The higher the magnification rate becomes, the coarser speed setting units tend to be. Normally set the magnification rate as low as possible.

The relationship between a value entered and the magnification rate is as follows.

$$\text{Speed magnification [times]} = \frac{\text{Reference clock frequency [Hz]}}{\text{RMG x 8192}}$$

Table 10-3 Magnification setting example (when reference clock frequency = 4.9152 [MHz])

Setting value	Speed magnifi-cation	Range of output speed (pps)
600 (258h)	1	1 ~ 8,191
300 (12Ch)	2	2 ~ 16,382
120 (078h)	5	5 ~ 40,955
60 (03Ch)	10	10 ~ 81,910
30 (01Eh)	20	20 ~ 163,820

Setting value	Speed magnifi-cation	Range of output speed (pps)
12 (00Ch)	50	50 ~ 409,550
6 (006h)	100	100 ~ 819,100
3 (003h)	200	200 ~ 1,638,200
2 (002h)	300	300 ~ 2,457,300
-	-	-

◆ RDP: Ramping-down point setting register (24-bit)

Specify a ramping-down point in high-speed (with acceleration / deceleration) positioning operation.
The definition of the value to be set in the RDP varies according to the setting status of RENV.ASDP (ramping-down point setting)

[Manual setting (RENV.ASDP=0)]

Specify a number of pulses from a ramping-down point to target position in the range of 0 ~ 16,777,215 (FFFFFFh).
The optimum value of a ramping-down point is as follows.

1. Linear acceleration / deceleration (Control mode command.CCM5=0)

$$\text{Optimum value [pulse]} = \frac{(RFH^2 - RFL^2) \times RUD}{RMG \times 16384}$$

2. S-curve acceleration / deceleration (Control mode command.CCM5=1)

$$\text{Optimum value [pulse]} = \frac{(RFH^2 - RFL^2) \times RUD}{RMG \times 8192}$$

At the timing of (number of remaining pulses for positioning) ≤ (a setting value in RDP), a motor starts to decelerate.

[Automatic setting (RENV.ASDP=1)]

Because the speed profile of acceleration characteristics and deceleration characteristics are symmetric, the LSI memorizes the number of pulses for acceleration and use the value as the automatic setting of a ramping-down point. The range of automatic setting value (number of pulses for acceleration) to operate correctly is 0 ~ 8,388,607(7FFFFFh).
The RDP setting value is an offset from automatic setting value and set in the range of -8,388,608 (800000h) ~ 8,388,607 (7FFFFFh).
When an offset amount is positive number, a motor starts deceleration earlier and operates at FL speed after deceleration is completes.
When an offset amount is negative number, a motor stops before the speed cannot reach to FL speed.
When offset is unnecessary, set "0".

10-2-1. Setting example of acceleration / deceleration pattern

When initial speed = 1000 [pps], operation speed = 10000 [pps], acceleration / deceleration time = 300 [msec] and feeding amount = 4000 [pulse] in S-curve acceleration / deceleration positioning operation, a setting value is calculated as follows. (Reference clock = 4.9152 [MHz])

1. Set Control mode command=64h (S-curve acceleration / deceleration positioning).
2. Set a feeding amount in RMV (RMV=4000).
3. To output 10000 [pps], set a speed magnification as 2x mode and RMG=300 (12Ch).
4. Set RFL=500 (1F4h) so as to set initial speed 1000 [pps] in 2x mode.
5. Set RFH=5000 (1388h) in RFH so as to set operation speed 10000 [pps] in 2x mode.
6. Calculate acceleration / deceleration rate (RUD) setting value using acceleration / deceleration time.

$$\text{Acceleration / deceleration time [s]} = \frac{(\text{RFH} - \text{RFL}) \times \text{RUD} \times 2}{\text{Reference clock frequency [Hz]}}$$

RUD = 0.3 [s] x 4,915,200 [Hz] / ((5000-500) x 2) = 163.84

A value in RUD is an integer. The nearest integer will be set to “164”.
Acceleration / deceleration time at the time is 300.29 [msec].

7. Set RDP = 0 in automatic ramping-down point setting (RENV.ASDP = 1).
   In manual setting (RENV.ASDP = 0), calculate a setting value in RDP as follows.

$$\text{A setting value in RDP} = \frac{(\text{RFH}^2 - \text{RFL}^2) \times \text{RUD}}{\text{RMG} \times 8192}$$

$$= \frac{(5000^2 - 500^2) \times 164}{(300 \times 8192)} = 1651.6$$

   By rounding the above value down to an integer, a setting value in RDP =1651.

8. High-speed start command (15h) is written.

10-3. Changing speed pattern in operation

By changing the RFL, RFH and RUD registers in operation, the speed and the rate of acceleration can be changed on the fly.

[Changing speed during a linear acceleration / deceleration]

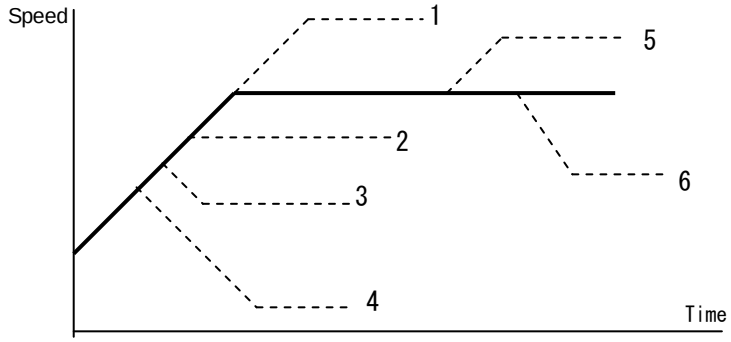


Figure 10-2 Changing speed pattern in operation (linear)

1. Make RFH larger during accelerating, the motor accelerates until the speed reaches the corrected speed. (Old speed < new speed)
2. Make RFH smaller during accelerating, the motor accelerates until the speed reaches the corrected speed and runs at constant speed. (Current speed < new speed < old speed)
3. Make RFH smaller during accelerating, the motor decelerates until the speed reaches the corrected speed. (RFL ≤ new speed < current speed)
4. Make RFH smaller during accelerating, the motor decelerates until the speed reaches the corrected speed. (New speed < RFL)
5. Make RFH larger after accelerating is complete, the motor accelerates until the speed reaches the corrected speed.
6. Make RFH smaller after accelerating is complete, the motor decelerates until the speed reaches the corrected speed.

[Changing speed during an S-curve acceleration / deceleration]

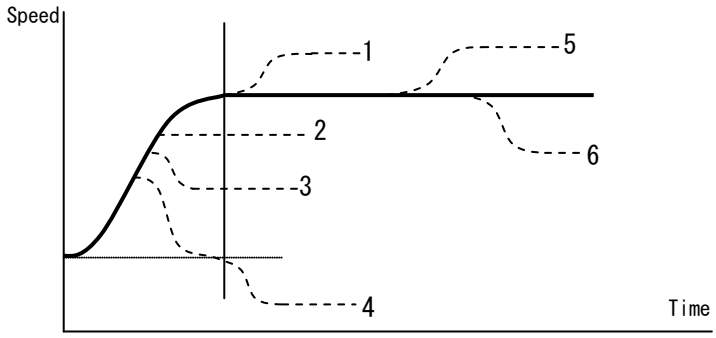


Figure 10-3 Changing speed pattern in operation (S-curve)

1. Make RFH larger during accelerating, the motor accelerates to the old speed and accelerates to the new speed again. (Old speed < new speed)
2. Make RFH smaller during accelerating, the motor accelerates until the speed reaches the corrected speed and operates at the constant speed. (Current speed < new speed < old speed)
3. Make RFH smaller during accelerating, the motor decelerates until the speed reaches the corrected speed. (RFL ≤ new speed < current speed)
4. Make RFH smaller during accelerating, the motor decelerates to the FL speed and decelerates to the new speed again. (New speed < RFL)
5. Make RFH larger after accelerating is complete, the motor accelerates until the speed reaches the corrected speed.
6. Make RFH smaller after accelerating is complete, the motor decelerates until the speed reaches the corrected speed.

10-4. Restriction of changing speed pattern in auto setting of ramping-down point

In the following cases, auto setting function of ramping-down point cannot follow.

- Change values in RFL and RUD registers
- Change RFH register value in S-curve acceleration / deceleration

Aside from the above, error of ramping-down point may be accumulated when RFH registers are changed several times in linear acceleration / deceleration.

11. Function description

11-1. Reset

This LSI is reset if longer than 3 clocks of reference clock are input with making RST terminal L level.
All registers and all output terminals status are not determined during the time between reset and power on.
After reset, the LSI becomes the default setting as follows.

Table 11-1 Default status at canceling reset

Description	Default	Condition
Start mode command	00h	-
Control mode command	40h	-
Register selection command	80h	-
Output mode command	C0h	With parallel I/F
	E0h	With serial I/F
Main status (MSTS)	37h	-
Register Write buffer (RegWBF)	000000h	-
Register Read buffer (RegRBF)	000000h	-
RMV, RFL, RFH, RUD, RMG, RDP, RIDL, RCUN, RIOP, RSPD registers	0h	-
RENV register	000000h	With parallel I/F
	000002h	With serial I/F
RSTS register (Extended status)	0x11 x001 1xxx xxxxb	-
RIDC register (Product information code)	98h	PCD4611A
	A8h	PCD4621A
	C8h	PCD4641A
RSPO register	00h	With parallel I/F
	00xx xxxxb	With serial I/F
RSPM register	00h	With parallel I/F
	3Fh	With serial I/F
D0 ~ D7 terminals	Hi-z	With parallel I/F
SP0 ~ SP5 terminals	Input terminal status	With serial I/F
INT, WRQ, +PO/PLS, -PO/DIR, BSY terminals	H level	-
OTS terminal	L level	-
PH1/P1, PH2/P2, PH3/P3, PH4/P4 terminals	H, L, L, H	U/B terminal = L
	H, L, L, L	U/B terminal = H

x: changes in input terminal.

11-2. Idling pulse output

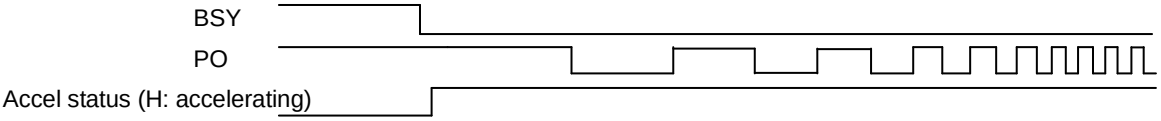
When a motor starts at FH high speed, it will normally accelerate right after starting. This LSI can make a motor start acceleration after outputting several pulses at FL speed.

Normally, the speed calculated from the initial output pulse cycle will be higher than the FL speed, a motor may not start automatically if the FL speed is set to approximately the auto start frequency. The idling pulse function enables to start acceleration after outputting some pulses at FL speed. Therefore, the motor can surely start from FL speed. The pulses output at FL speed are referred to as “idling pulses” and number of pulses is set to in the RIDL register.

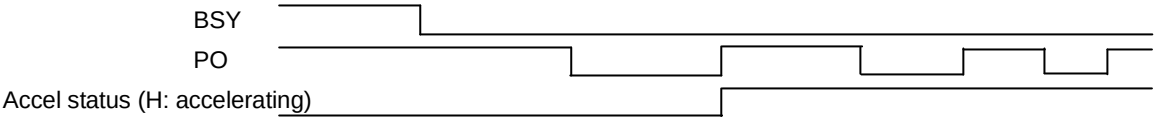
The allowable range is 0 ~ 7 and this mode is available in high-speed operation (with acceleration / deceleration). When this is set to 0, the motor will make a normal start.

The timing when output pulse train (PO) is output in negative logic is as follows.

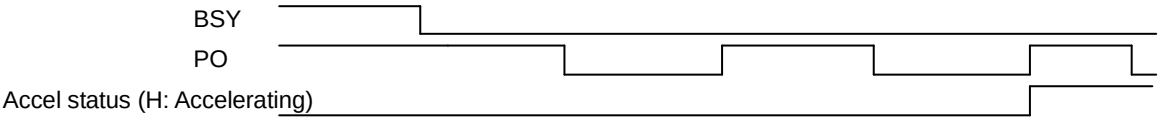
● When RIDL = 0



● When RIDL = 1



● When RIDL = 2



11-3. External start control

This LSI can be started using an external signal (STA signal).
Multiple axes can be started simultaneously.

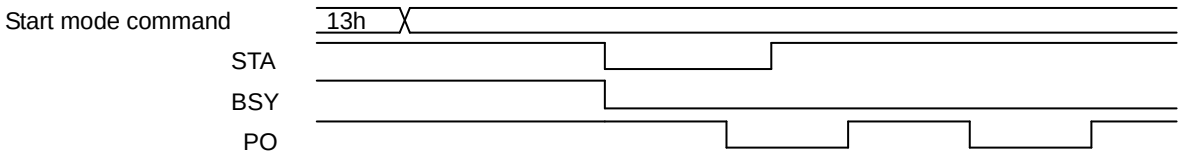
Make Start mode command.SCM1 = 1 and write a start command with holding start.
After that hold is released at the falling edge of STA terminal, the motor starts.
To cancel the hold, an immediate stop command can also be used.
Input an STA signal whose width is longer than 4 reference clock cycles.

During "Holding the start", if an STP or EL signal of the same direction as operation, or ORG signals (Control command.CCM0=1) are input, the LSI will store the stop condition internally, and the LSI will not start operation even if an STA signal is input.
Operation changes as follows by compatible mode setting.

- In PCD46x1 mode, though STA signal is input in holding stop status, operation does not occur. Holding stop status is cancelled and status becomes “stopped”. When a start command is written, operation starts. Stop interrupt occurs when holding stop status.
- In PCD45x1 compatible mode and PCD4500 compatible mode, even though STA signal and a start command is input with holding stop status, operation does not occur. Holding stop status is released and status becomes “stopped”. This time, stop interrupt and STA interrupt occur.

When status is “stopped”, start control bits (SCM4) of start mode monitor in buffer (bits 23 ~ 16) to read out register changes “1” to “0”. About the above operation, see “11-11-6. Timing to stop hold start.

- Start timing (FH constant speed holding start)



11-4. External stop control

This LSI can be stopped using an external signal. With this function, you can stop a motor in an emergency and use to stop multiple axes simultaneously.

When the STP terminal goes L level, the motor will stop immediately or decelerate and stop.
The motor stops immediately with RENV.SPDS=0 and decelerates and stops with RENV.SPDS=1.

While STP terminal is L level, the LSI does not output any pulses and operation is completed even though a start command is written.
In even this case, INT signal can be output at stopping.
A filter can be applied to this signal by the setting of Output mode command.OCM4
This filter removes noises that are shorter than 3 cycles of reference clock. Therefore, if a filter is applied, input pulses that have pulse width that is more than 4 cycles of reference clock (approximately 800[ns] at 4.9152[MHz]). Without filters, this LSI accepts pulse signals that have pulse width less than 800 [ns]. Selection to apply filter is common among ORG, +EL, -EL, STP signals.

11-5. Output pulse mode

There are 2-pulse mode and common pulse mode in output pulse mode and they can be selected by RENV.PMD.
With RENV.PMD=0, 2-pulse mode is selected, the LSI outputs pulse train signals from terminal (+PO / PLS) in (+) direction operation and from terminal (-PO / DIR) in (-) direction operation.
With RENV.PMD=1, common pulse mode is selected. The LSI outputs pulse train signals from terminal (+PO / PLS) and direction signals from terminal (-PO / DIR).
The logic of output signals can be selected by Output mode command.OCM0.

Table 11-2 Output pulse mode

PMD	OCM0	In [+] direction operation	In [-] direction operation
0	0	+PO -PO H	+PO H -PO
0	1	+PO -PO L	+PO L -PO
1	0	PLS DIR H	PLS DIR L
1	1	PLS DIR L	PLS DIR H

11-6. Excitation sequence output

This LSI can generate 2-2 phase and 1-2 phase excitation sequences for 2-phase stepper motors to provide unipolar and bipolar driving.

Excitation sequence signals are output from four PH1 / P1, PH2 / P2, PH3 / P3, PH4 / P4 terminals.
These 4 terminals are also used as general-purpose input and output port terminals. When these are used to output excitation sequence signals, set RENV.IOPM=0.

Switch between unipolar driving and bipolar driving is made by U/B terminal. This setting latches the setting level with RST = L. Therefore, this LSI should be reset after setting change.

Switch between 2-2 phase excitation and 1-2 phase excitation is made by F/H terminal.
Because this setting is not latched, you can switch them during operation.

When switching to 2-2 phase excitation at 1 phase excitation in 1-2 phase excitation (STEP 1,3,5,7 in 1-2 phase excitation in below Table 11-3 and 11-4), the next output pulse is in 2 phase excitation

Table 11-3 Unipolar excitation sequence (U/B = L)

2-2 phase excitation (F/H=L)					
STEP	0	1	2	3	0
PH1	H	H	L	L	H
PH2	L	H	H	L	L
PH3	L	L	H	H	L
PH4	H	L	L	H	H
SPHZ	H	L	L	L	H
[-]←Operation direction →[+]					

1-2 phase excitation (F/H=H)									
STEP	0	1	2	3	4	5	6	7	0
PH1	H	H	H	L	L	L	L	L	H
PH2	L	L	H	H	H	L	L	L	L
PH3	L	L	L	L	H	H	H	L	L
PH4	H	L	L	L	L	L	H	H	H
SPHZ	H	L	L	L	L	L	L	L	H
[-] ← Operation direction → [+]									

Table 11-4 Bipolar Excitation sequence (U/B = H)

2-2 phase excitation (F/H=L)					
STEP	0	1	2	3	0
PH1	H	H	L	L	H
PH2	L	H	H	L	L
PH3	L	L	L	L	L
PH4	L	L	L	L	L
SPHZ	H	L	L	L	H
[-]← Operation direction →[+]					

1-2 phase excitation (F/H=H)									
STEP	0	1	2	3	4	5	6	7	0
PH1	H	H	H	H	L	L	L	L	H
PH2	L	L	H	H	H	H	L	L	L
PH3	L	L	L	H	L	L	L	H	L
PH4	L	H	L	L	L	H	L	L	L
SPHZ	H	L	L	L	L	L	L	L	H
[-] ← Operation direction → [+]									

Note

- SPHZ means RSTS.SPHZ and it is excitation origin monitor signal to be confirmed as status.
- With output mode command.OCM2 = 1, all PH1 ~ PH4 outputs are fixed as follows.

  (RENV.MSKM = 0): PH1 = L, PH2 = L, PH3 = L, PH4 = L

  (RENV.MSKM = 1): PH1 = L, PH2 = L, PH3 = H, PH4 = H

[Timing to change excitation sequence]

When pulse train output signal changes from ON to OFF, a sequence signal changes.

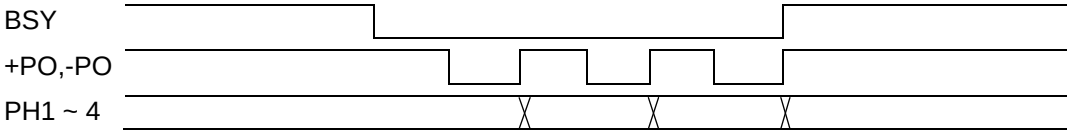


Figure 11-1 Timing when excitation sequence changes

Table 11-5 Excitation sequence output setting items

Mask of excitation sequence signal <OCM2> 0: Outputs sequence signal from PH1 ~ 4 terminals. 1: Masks sequence output of PH1 ~ 4 terminals.	Output mode command (WRITE) 7 0 - - - - - n - -
Output setting when excitation sequence output is masked. <RENV.MSKM> (Enable only when Output mode command.OCM2 = 1.) 0: PH1 = L, PH2 = L, PH3 = L, PH4 = L 1: PH1 = L, PH2 = L, PH3 = H, PH4 = H	RENV register (WRITE) 7 0 - - - - - n - -
Excitation origin point monitor <RSTS.SPHZ> 0: Sequence output (PH1 ~ 4) step is not excitation origin point. 1: Sequence output (PH1 ~ 4) step is excitation origin point.	RSTS register (READ) 7 0 n - - - - - - -
Excitation sequence signal monitor <RSTS.SPH1 ~ SPH4> Bit 11:PH4, bit 10: PH3, bit 9: PH2, bit 8 PH1 0: L level 1: H level	RSTS register (READ) 15 8 - - - - n n n n

11-7. Mechanical external input control

The LSI receives the following 5 signals (3 systems) as position detection signals from mechanical system.

Table 11-6 Mechanical external input signals

System	Signal
End limit detection signal	+EL, -EL
Ramping-down point detection signal	+SD, -SD
Origin point signal	ORG

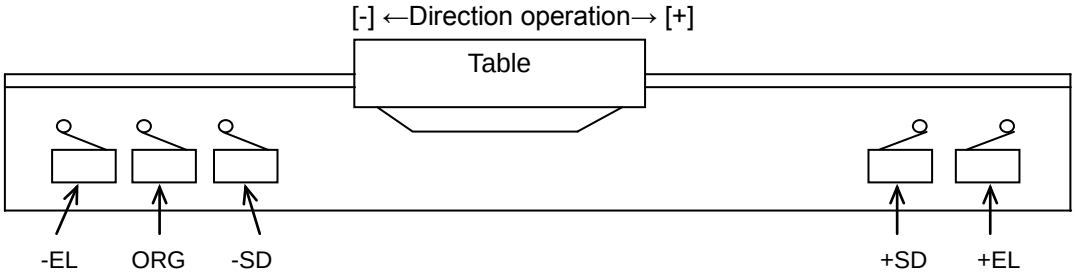


Figure 11-2 An example of mechanical external input control

11-7-1. End limit detection signal

When an EL signal of the same direction as operation (+EL signal in [+] direction operation) becomes L level, the motor stops immediately or decelerates and stops (selected by RENV.ELDS) and remains stopped even though this signal returns to H level.

If motor operates with start mode command.SCM5 = 1, INT signal can be output when the motor stops by this signal.

While this signal is L level, the motor does not start in the same direction as this signal even if a start command is input. However, INT signal is output.

Pulse output is masked with Output mode command.OCM = 1, EL signal becomes disabled. However you can monitor these signals' status (RSTS.SPEL, RSTS.SMEL).

A filter can be applied to this signal by Output mode command.OCM4. This filter removes noises that are shorter than 3 cycles of reference clock. Therefore, when a filter is applied, input pulses that are longer than 4 cycles of reference clock (approximately 800[ns] at 4.9152[MHz]. Without filter, the LSI accepts even signals that are shorter than 800[ns]. The selection to apply filter is common among ORG, +EL, -EL and STP signals

11-7-2. Ramping-down point detection signal

When SD signal control is enabled with Control mode command.CCM1 = 1 and if SD signal of the same direction as operation becomes L level, the motor starts decelerating. Then, the motor accelerates again if the SD signal returns H level.

When this signal is L level with SD signal control enabled, the motor does not accelerate and operates FL speed in spite of writing high speed start command. SD signal in decelerating is disabled.

Regardless of the setting of Control mode command.CCM1, you can monitor these signals' status (RSTS.SPSD, RSTS.SMSD).

11-7-3. Origin point signal

When ORG signal control is enabled (origin return operation) with Control mode command.CCM0 = 1 and this signal becomes L level, the motor stop immediately or decelerates and stops (selected by RENV.ORDS) and remains stopped even though this signal returns to H level.

With Start mode command.SCM5 = 1, INT signal can be output when the motor stops by this signal.

While this signal is L level, the motor does not start in the same direction as this signal even if a start command is input. However, INT signal is output.
Regardless of the setting of Control mode command.CCM0, you can monitor these signals' status (RSTS.SORG).
Pulse output is masked with Output mode command.OCM, ORG signal becomes disabled. However, you can monitor this signal's status (RSTS.SORG). Just like EL and STP signals, filter can be applied to this signal.

11-8. Interrupt request signal output

This LSI can output an INT signal when the motor stops, when passing the ramping-down point, or when an external start signal is received.
To output an interrupt request signal when the motor stops, use Start mode command.SCM5.
To output an interrupt request signal when passing a ramping-down point, use Register selection command.RCM4.
To output an interrupt request signal when an external start signal is received, use Register selection command.RCM5.
By setting each interrupt control bit to "1," INT signal will be output at each situation that is selected.
To reset INT factor, place "0" in respective control bit. When all INT factors are cleared, INT signal is cleared.
If you want interrupt factors not to occur when conditions are met, place "0" in respective control bit.
When any interrupt cause occurs among the control bits you set to "1", INT signal is output. To determine which interrupt cause occurs, check with main status (MSTS.ISTP, MSTS.ISDP and MSTS.ISTA).
The output status of an INT signal can be check with extended status (RSTS.SINT).

To use this terminal, connect to a pull up resistor (5 K ~ 10 K ohm) externally. In the case that several LSIs are used, INT terminals can be connected with one another in Wired-OR connection.

[How to use interrupt at passing a ramping-down point]

Comparing with a down counter value (RMV) and a passing ramping-down value (SDP), the LSI will output an INT signal when RMV ≤ SDP.

When a ramping-down point is set as manual (RENV.ASDP=0), SDP value = RDP setting value.
Only in positioning operation with high-speed start, a motor starts deceleration with RMV ≤ SDP.
Therefore, to operate positioning operation at constant speed, this can be used as a comparator for remaining pulses.

Table 11-7 Interrupt output setting terms

Interrupt control when a motor stops <SCM5> 0: Does not output INT signal when a motor stops. (This INT factor is cleared.) 1: Outputs INT signal when a motor stops.	Start mode command (WRITE) 7 0 0 0 n - - - - -
Interrupt control at passing a ramping-down point <RCM4> 0: Does not output INT signal at passing ramping-down point. (This INT factor is cleared.) 1: Output INT signal at passing ramping-down point.	Register selection command (WRITE) 7 0 1 0 - n - - - -
Interrupt control at the external start <RCM5> 0: Does not INT signal at external start. (This INT factor is cleared.) 1: Outputs INT signal at external start.	Register selection command (WRITE) 7 0 1 0 n - - - - -
Interrupt signal output monitor <RSTS.SINT> 0: All of ISTP, ISDP and ISTA in MSTS are OFF. 1: Either of ISTP, ISDP or ISTA in MSTS is ON.	RSTS register (READ) 15 8 n - - - - - - -

Interrupt monitor when a motor stops <MSTS.ISTP> 0: Outputting INT signal by stopping. 1: Does not output INT signals by stopping.	Main status (READ) 7 0 - - - - - - - n
Interrupt monitor at passing ramping-down point <MSTS.ISDP> 0: Outputting INT signals at passing ramping-down point 1: Does not output INT signal at passing ramping-down point	Main status (READ) 7 0 - - - - - - n -
Interrupt monitor at the external start <MSTS.ISTA> 0: Outputting INT signal by external start. 1: Does not output INT signal by external start.	Main status (READ) 7 0 - - - - - n - -

11-9. General-purpose ports

11-9-1. OTS terminal

This is a terminal for only general-purpose output ports.

Output status can be changed by Control mode command.CCM4.

Table 11-8 OTS terminal setting items

OTS terminal level control <CCM4> 0: Makes OTS terminal L level. 1: Makes OTS terminal H level.	Control mode command (WRITE) 7 0 0 1 - n - - - -

11-9-2. U/B, F/H terminals

This is an input terminal to set excitation sequence output method.

These terminals' input status can be monitored by RIOP.MUB and RIOP.MFH.

When excitation sequence output signals are not used, they can be used as general-purpose input ports.

In PCD45x1 compatible mode and PCD4500 compatible mode. This terminal cannot be used as general-purpose port because RIOP register cannot be accessed.

Table 11-9 U/B, F/H terminals setting items

U/B terminal level monitor <RIOP.MUB> 0: U/B terminal is L level 1: U/B terminal is H level	RIOP register (READ) 7 0 0 0 - n - - - -
F/H terminal level monitor <RIOP.MFH> 0: F/H terminal is L level. 1: F/H terminal is H level.	RIOP register (READ) 7 0 0 0 n - - - - -

11-9-3. P1 ~ P4 terminals

These 4 terminals are for both excitation sequence signals (PH1 ~ PH4) and general-purpose input / output ports.

Input terminals of excitation sequence signal (PH1 ~ PH4) or general–purpose input / output ports are selected by setting of RENV.IOPM. These terminals are output terminals of excitation sequence output at default setting.

When using as general-purpose input / output ports (P1 ~ P4) (RENV.IOPM = 1), RENV register (RENV.IPM1 ~ IPM4) is used to switch between general-purpose input and general-purpose output and to monitor output status and terminal status by RIOP register.

In PCD45x1 compatible mode and PCD4500 compatible mode, these terminals cannot be used as general-purpose input port because RIOP register cannot be accessed.

It is possible to independently switch each terminal between general-purpose input and general-purpose output

Even when general-purpose output port is selected, you can monitor terminal level.

At default setting, these are PH1 ~ PH4 output terminals.

[Note] To use general-purpose input terminals, there are precautions. Please refer to "14-1-6 When general-purpose input / output ports (P1 ~ P4) are used as general-purpose input" in detail.

Table 11-10 P1 ~ P4 terminal setting items

Select functions of P1 ~ P4 terminals <RENV.IOPM> 0: Output terminals of excitation sequence signals (PH1 ~ PH4) 1: General-purpose input / output port (P1 ~ P4)	RENV register (WRITE) 15 8 - - - - n - - -
Specification selections of P1 general-purpose input / output terminal <RENV.IPM1> 0: P1 terminal is general-purpose output terminal 1: P1 terminal is general-purpose input terminal	RENV register (WRITE) 15 8 - - - n - - - -
Specification selections of P2 general-purpose input / output terminal <RENV.IPM2> 0: P2 terminal is general-purpose output terminal 1: P2 terminal is general-purpose input terminal	RENV register (WRITE) 15 8 - - n - - - - -
Specification selections of P3 general-purpose input / output terminal <RENV.IPM3> 0: P3 terminal is general-purpose output terminal 1: P3 terminal is general-purpose input terminal	RENV register (WRITE) 15 8 - n - - - - - -
Specification selections of P4 general-purpose input / output terminal <RENV.IPM4> 0: P4 terminal is general-purpose output terminal 1: P4 terminal is general-purpose input terminal	RENV register (WRITE) 15 8 n - - - - - - -
Monitor general-purpose input / output terminal level <RIOP.CP4 ~ CP1> Bit 0: P1 terminal monitor Bit 1: P2 terminal monitor Bit 2: P3 terminal monitor Bit 3: P4 terminal monitor	RIOP register (READ) 7 0 0 0 - - n n n n
Output setting of general-purpose output terminal (0: L level、1: H level) <RIOP.CP4 ~ CP1> Bit 0: P1 output level Bit 1: P2 output level Bit 2: P3 output level Bit 3: P4 output level	RIOP register (WRITE) 7 0 0 0 - - n n n n

11-10. Common ports

11-10-1. SP0 ~ SP5 terminals

These are common ports (Shared ports) that can be used as general-purpose input / output ports with serial I/F. While there are general-purpose ports P1 ~ P4 terminals per axis, there is one set of common ports SP0 ~ SP5 in each LSI regardless of number of axes.

General-purpose input or general-purpose output are switched by RSPM and output status and terminal status are monitored by RSP0.

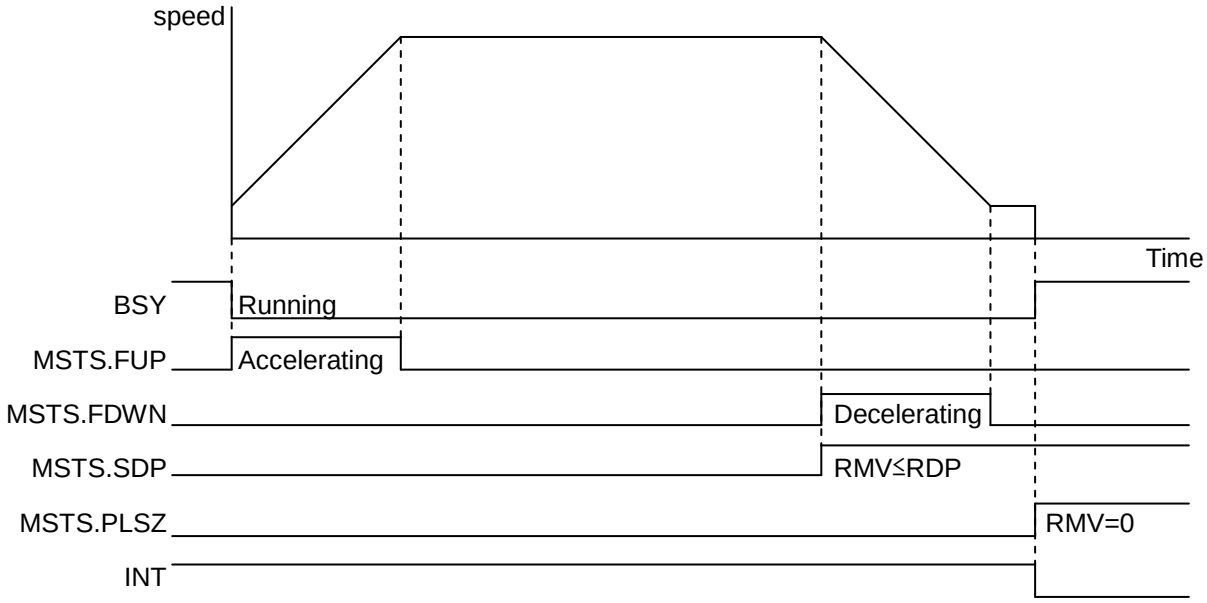
At default status, all are general-purpose input signals

Table 11-11 SP0 ~ SP5 terminal setting items

Specification selection of SP0 common input / output terminal<RSPM.SPM0> 0: SP0 terminal is general-purpose output terminal 1: SP0 terminal is general-purpose input terminal	RSPM register (WRITE) 7 0 - - - - - - - n
Specification selection of SP1 common input / output terminal<RSPM.SPM1> 0: SP1 terminal is general-purpose output terminal 1: SP1 terminal is general-purpose input terminal	RSPM register (WRITE) 7 0 - - - - - - n -
Specification selection of SP2 common input / output terminal<RSPM.SPM2> 0: SP2 terminal is general-purpose output terminal 1: SP2 terminal is general-purpose input terminal	RSPM register (WRITE) 7 0 - - - - - n - -
Specification selection of SP3 common input / output terminal<RSPM.SPM3> 0: SP3 terminal is general-purpose output terminal 1: SP3 terminal is general-purpose input terminal	RSPM register (WRITE) 7 0 - - - - n - - -
Specification selection of SP4 common input / output terminal<RSPM.SPM4> 0: SP4 terminal is general-purpose output terminal 1: SP4 terminal is general-purpose input terminal	RSPM register (WRITE) 7 0 - - - n - - - -
Specification selection of SP5 common input / output terminal<RSPM.SPM5> 0: SP5 terminal is general-purpose output terminal 1: SP5 terminal is general-purpose input terminal	RSPM register (WRITE) 7 0 - - n - - - - -
Level monitor of common terminals <RSPO.SPO5 ~ SPO0> Bit 0: SP0 terminal monitor Bit 1: SP1 terminal monitor Bit 2: SP2 terminal monitor Bit 3: SP3 terminal monitor Bit 4: SP4 terminal monitor Bit 5: SP5 terminal monitor	RSPO register (READ) 7 0 0 0 n n n n n n
Control of general-purpose output terminal (0: L level、1: H level) <RSPO.SPO5 ~ SPO0> Bit 0: SP0 output level Bit 1: SP1 output level Bit 2: SP2 output level Bit 3: SP3 output level Bit 4: SP4 output level Bit 5: SP5 output level	RSPO register (WRITE) 7 0 0 0 n n n n n n

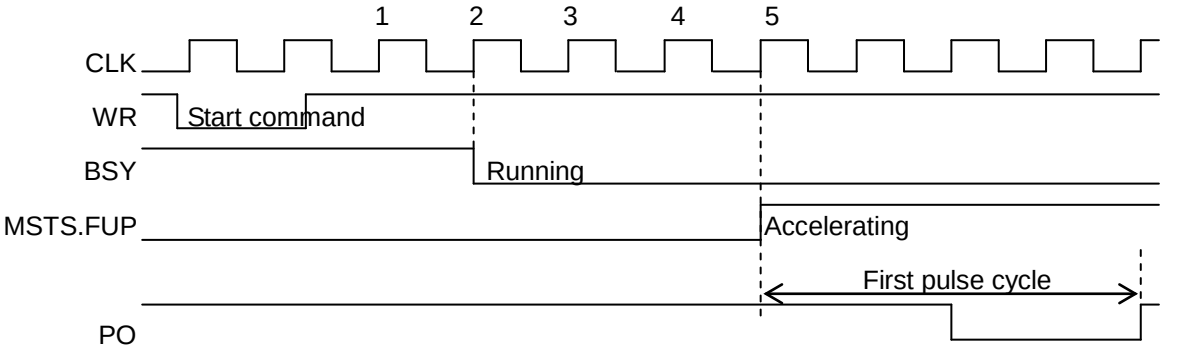
11-11. Operation timing

11-11-1. Acceleration / deceleration operation timing (positioning operation)

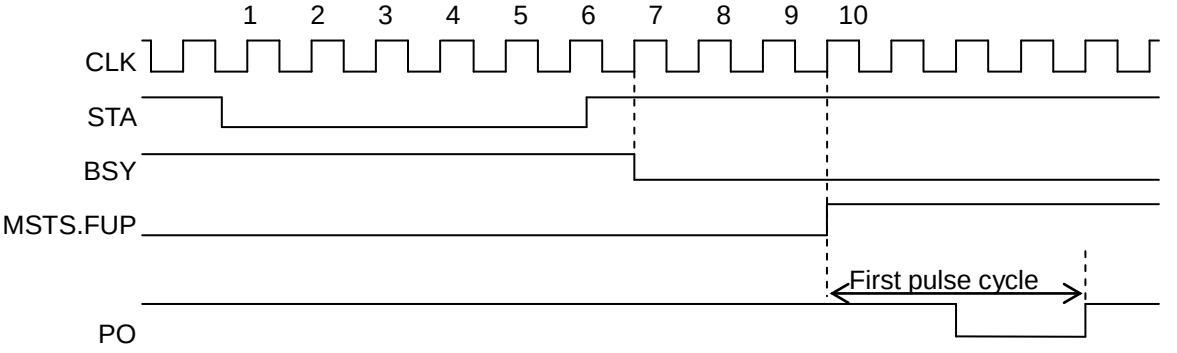


11-11-2. Start timing

11-11-2-1. Command start timing

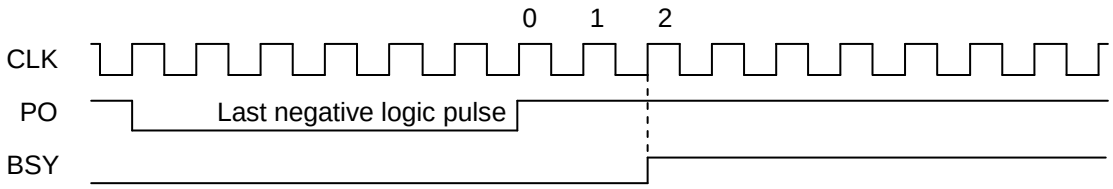


11-11-2-2. External start timing

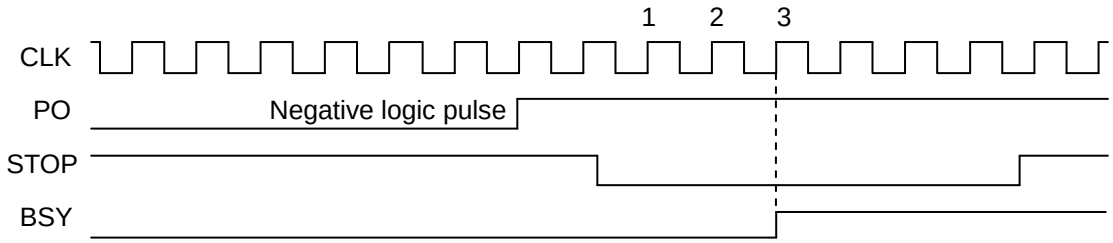


11-11-3. Stop timing

11-11-3-1. Positioning operation complete timing



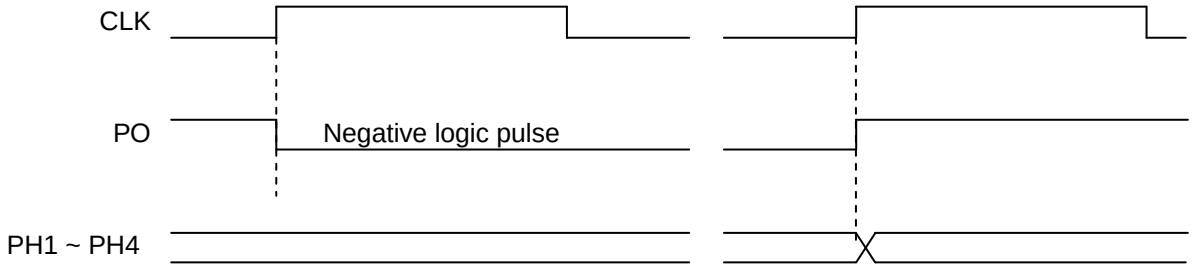
11-11-3-2. Stop timing by STP, ORG, EL signal input



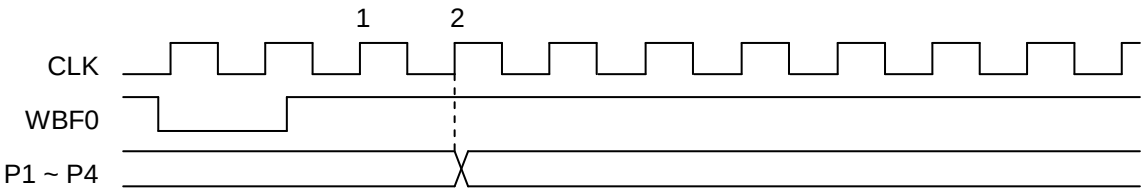
[Note]

1. STOP is a virtual signal. Stop = L level only when either STP, ORG, +EL or –EL is L level.
2. When a filter is applied with output mode command.OCM4 = 1, rising of BSY delays for 4 CLK cycles than the above figure.
3. When Stop becomes L level during PO is ON (H level), BSY rises when PO turns OFF (L level.

11-11-4. Pulse output, sequence output timing



11-11-5. General-purpose port output timing

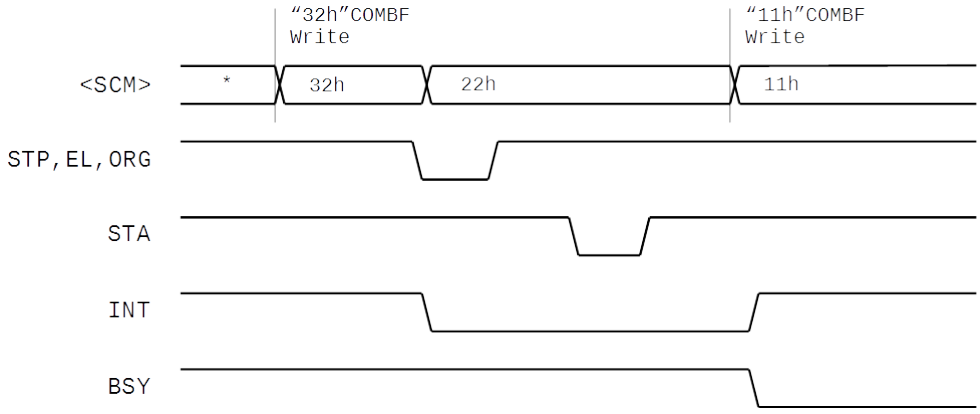


[Note] WBF0 is a virtual signal and a WR signal when the LSI writes to RegWBF(7~0) after RIOP is selected by Register selection command.

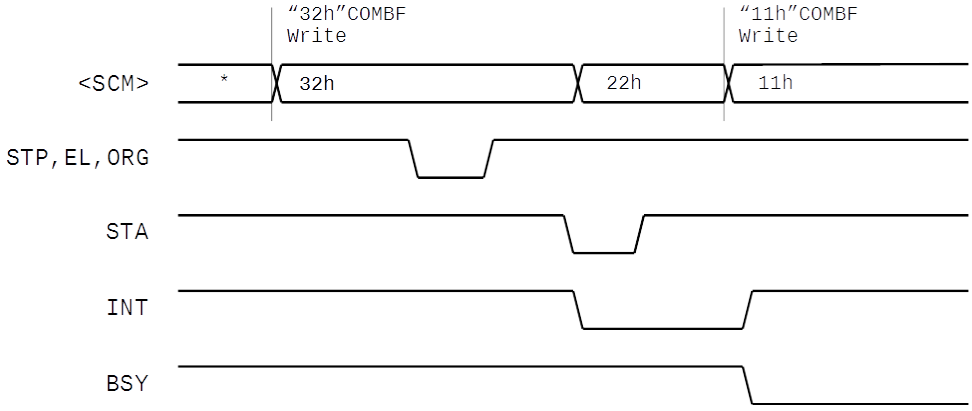
11-11-6. Timing to stop holding start

11-11-6-1. STA signal input after stopping holding start

PCD46x1 mode



PCD45x1 compatible mode and PCD4500 compatible mode



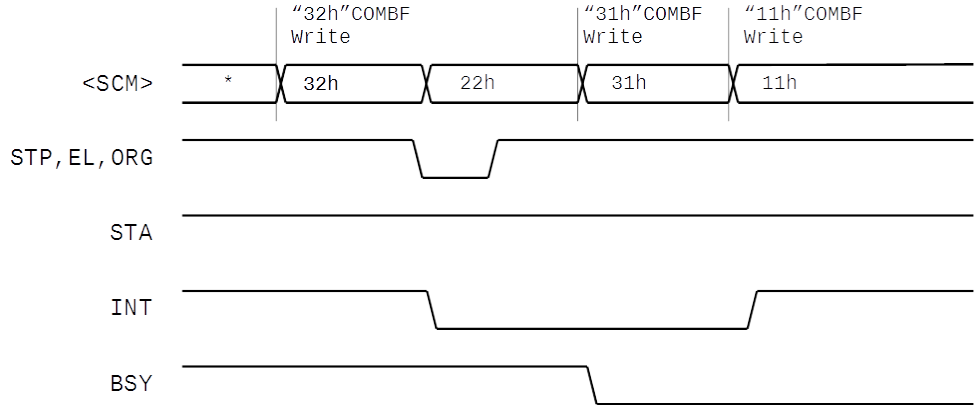
[Note]

Stop by ORG signal input is in the case of Control mode command.CCM0 = 1.

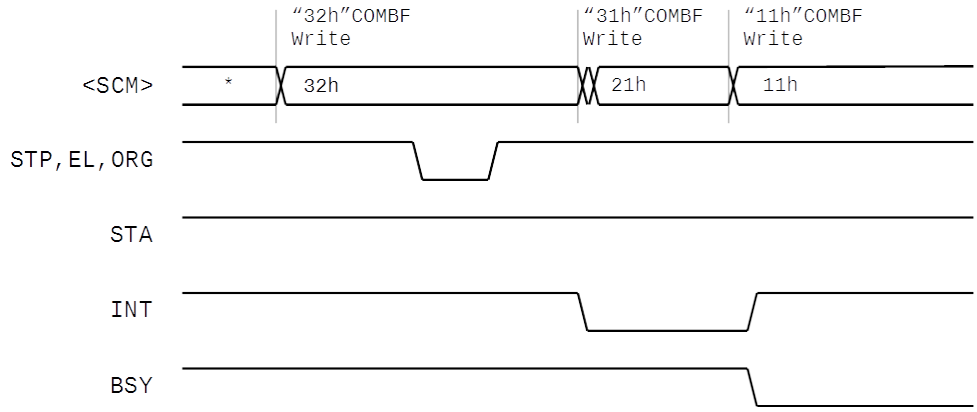
INT signal is output L level when INT output is set to be enabled as a triggered condition.

11-11-6-2. Writing start command after stopping holding start

PCD46x1 mode



PCD45x1 compatible mode and PCD4500 compatible mode



[Note]

Stop by ORG signal input is in the case of Control mode command.CCM0 = 1.

INT signal is output L level when INT output is set to be enabled as a triggered condition.

12. Electric characteristics

12-1. Absolute maximum rating

These are common values among PCD4611A, PCD4621A and PCD4641A.

Table 12-1 PCD46x1A absolute maximum rating

Item	Symbol	Rating	Unit
Power supply voltage	V_{DD}	-0.3 ~ +4.0	V
Input voltage	V_{IN}	-0.3 ~ +7.0	V
Current consumption	I_{OUT}	±30	mA
Storage temperature	T_{stg}	-65 ~ +150	℃

12-2. Recommended operating conditions

These are common values among PCD4611A, PCD4621A and PCD4641A.

Table 12-2 PCD46x1A recommended operating conditions

Item	Symbol	Rating	Unit
Power supply voltage	V_{DD}	+3.0 ~ +3.6	V
Input voltage	V_I	-0.3 ~ +5.8	V
Ambient temperature	T_a	-40 ~ +85	℃

12-3. DC characteristics (in recommended operating conditions)

These are common values among PCD4611A, PCD4621A and PCD4641A.

Table 12-3 DC characteristics (in recommended operating conditions)

Item	Symbol	Conditions	Min	Typ	Max	Unit
Static consumption current	I_{DDS}	$V_I=V_{DD}$ or GND, V_{DD}=Max, no negative load	-	-	35	µA
Consumption current	I_{DD}	PCD4611A ∗1	-	-	3	mA
		PCD4621A ∗1	-	-	5	
		PCD4641A ∗1	-	-	10	
		PCD4611A ∗2	-	-	6	mA
		PCD4621A ∗2	-	-	10	
		PCD4641A ∗2	-	-	20	
Input leakage current	I_{LI}	V_{DD}=Max, V_{IH}=VDD,V_{IL}=GND ∗3	-1	-	+1	µA
		V_{DD}=Max, V_I=GND ∗4	-90	-	-	
		V_{DD}=Min, V_{IH}=5.5V	-	-	30	
High input voltage	V_{IH}	V_{DD}=Max	2.0	-	5.8	V
Low input voltage	V_{IL}	V_{DD}=Min	-0.3	-	0.8	V
High output voltage	V_{OH}	V_{DD}=Min, I_{OH}=-6mA	V_{DD} - 0.4	-	-	V
Low output voltage	V_{OL}	V_{DD}=Min, I_{OL}=6mA	-	-	0.4	V
High output current	I_{OH}	V_{DD}=Min, $V_{OH}=V_{DD}$-0.4V	-	-	-6	mA
Low output current	I_{OL}	V_{DD}=Min, V_{OL}=0.4V	-	-	6	mA
Internal pull up resistance	R_{PU}	$V_I=V_{DD}$ or GND ∗4	40	100	240	K ohm
Input capacitance	C_I	f=1MHz, V_{DD}=GND	-	-	10	pF
Output terminal capacitance	C_O	f=1MHz, V_{DD}=GND	-	-	10	pF
Input / output terminal capacitance	C_{IO}	f=1MHz, V_{DD}=GND	-	-	10	pF

∗1: CLK=4.9152 MHz, when all axes operates at maximum speed (2.457 Mpps). (All output terminals have no load.)

∗2: CLK=10.000 MHz, when all axes operates at maximum speed (4.999 Mpps). (All output terminals have no load.)

∗3: D0 ~ D7, A0 ~ A3, RD, WR, CS, CLK terminals

∗4: ORG, +EL, -EL, +SD, -SD, STA, STP, U/B, F/H, RST terminals.

12-4. AC characteristics

12-4-1. Reference clock

These are common values among PCD4611A, PCD4621A and PCD4641A.

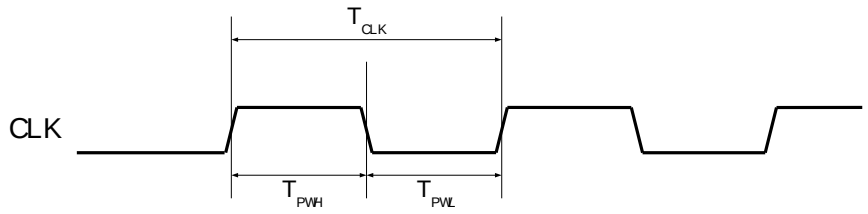


Figure 12-1 AC characteristics reference clock waveform

Table 12-4 AC characteristics reference clock

Item	Symbol	Conditions	Min	Max	Unit
Reference clock frequency	F_{CLK}	-	-	10	MHz
Reference clock cycle	T_{CLK}	-	100	-	ns
Reference clock HIGH width	T_{PWH}	-	40	-	ns
Reference clock LOW width	T_{PWL}	-	40	-	ns

12-4-2. Reset cycle

These are common values among PCD4611A, PCD4621A and PCD4641A.

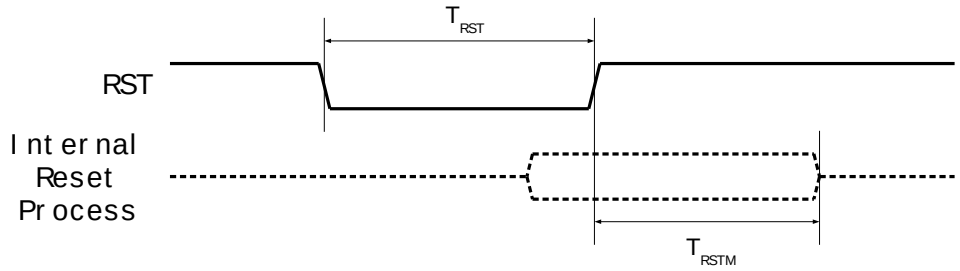


Figure 12-2 AC characteristics reset cycle waveform

Table 12-5 AC characteristics reset cycle

Item	Symbol	Conditions	Min	Max	Unit
RST signal width	T_{RST}	-	T_{CLK}×3	-	ns
Reset processing time	T_{RSTM}	-	T_{CLK}×3	T_{CLK}×4	ns

12-4-3. Parallel I/F read access

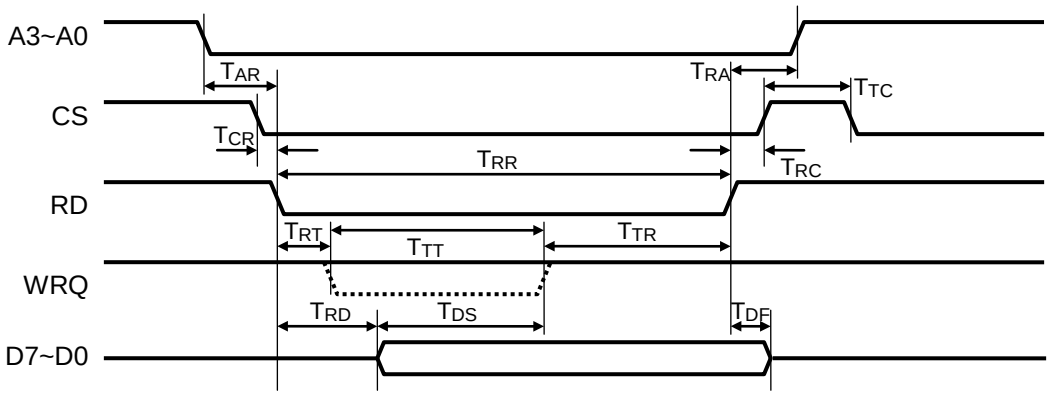


Figure 12-3 AC characteristics parallel I/F read access waveform

Table 12-6 AC characteristics parallel I/F read access

Item	Symbol	Condition	PCD4611A		PCD4621A		PCD4641A		Unit
			Min	Max	Min	Max	Min	Max	
Address set up time for RD↓	T_{AR}	-	0	-	0	-	0	-	ns
Address hold time for RD↑	T_{RA}	-	0	-	0	-	0	-	ns
RD signal width	T_{RR}	-	29	-	28	-	32	-	ns
CS set up time for RD↓	T_{CR}	-	0	-	0	-	0	-	ns
CS hold time for RD↑	T_{RC}	-	0	-	1	-	0	-	ns
WRQ on delay time for RD↓	T_{RT}	C_L=40pF	-	29	-	31	-	32	ns
WRQ on time	T_{TT}	-	-	T_{CLK}×3	-	T_{CLK}×3	-	T_{CLK}×3	ns
RD hold time	T_{TR}	-	0	-	0	-	0	-	ns
Data output delay time for RD↓	T_{RD}	C_L=40pF	-	29	-	31	-	32	ns
Data output pre cursor time	T_{DS}	C_L=40pF	0	-	0	-	0	-	ns
Data float time for RD↑	T_{DF}	C_L=40pF	-	22	-	22	-	22	ns
CS signal width	T_{TC}	-	10	-	10	-	10	-	ns

12-4-4. Parallel I/F write access

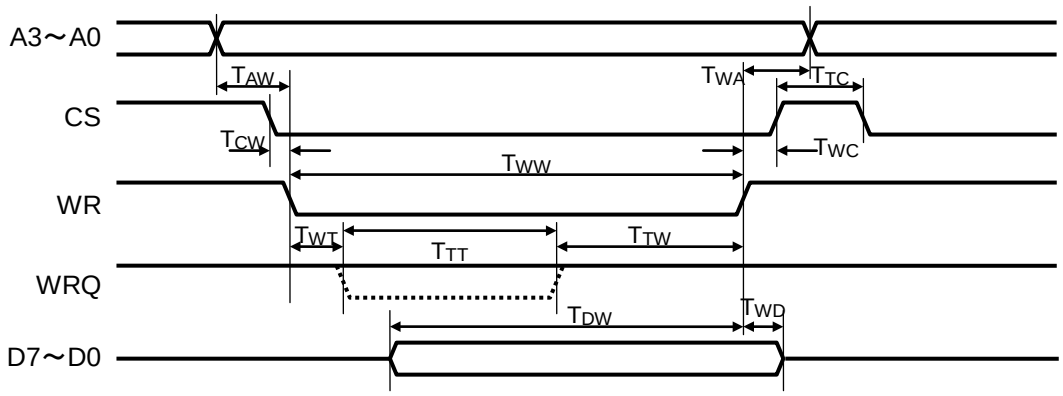


Figure 12-4 AC characteristics parallel I/F write access waveform

Table 12-7 AC characteristics parallel I/F write access

Item	Symbol	Conditions	PCD4611A		PCD4621A		PCD4641A		Unit
			Min	Max	Min	Min	Max	Min	
Address set up time for WR↓	T_{AW}	-	0	-	0	-	0	-	ns
Address hold time for WR↑	T_{WA}	-	0	-	0	-	0	-	ns
WR signal width	T_{WW}	-	16	-	17	-	16	-	ns
CS set up time for WR↓	T_{CW}	-	0	-	0	-	0	-	ns
CS hold time for WR↑	T_{WC}	-	1	-	1	-	0	-	ns
WRQ ON delay time for WR↓	T_{WT}	C_L=40pF	-	13	-	17	-	16	ns
WRQ ON time	T_{TT}	-	-	T_{CLK}×3	-	T_{CLK}×3	-	T_{CLK}×3	ns
WR hold time	T_{TW}	-	0	-	0	-	0	-	ns
CS signal width	T_{TC}	-	10	-	10	-	10	-	ns
Data set up time for WR↓	T_{DW}	-	13	-	14	-	13	-	ns
Data hold time for WR↑	T_{WD}	-	0	-	0	-	0	-	ns

12-4-5. Serial I/F access

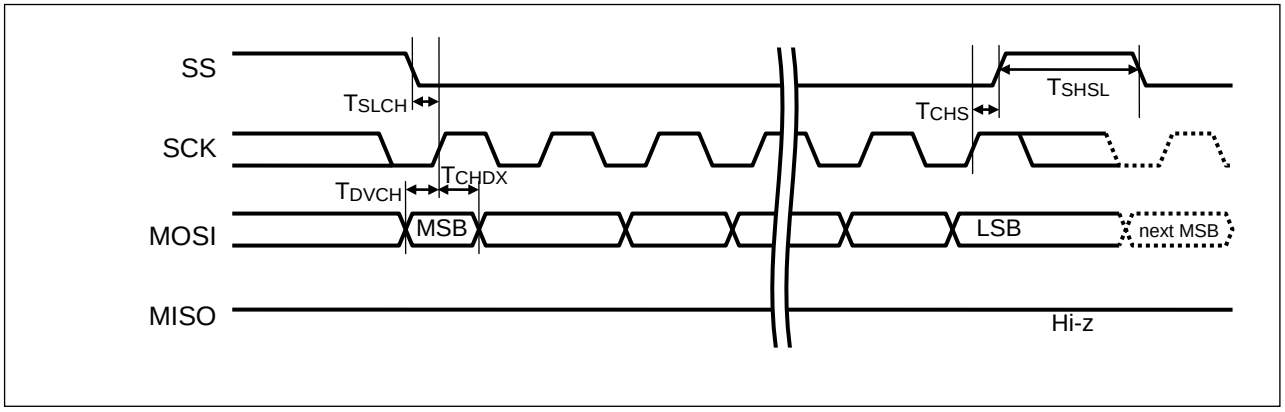


Figure 12-5 The head part of serial I/F write cycle / read cycle

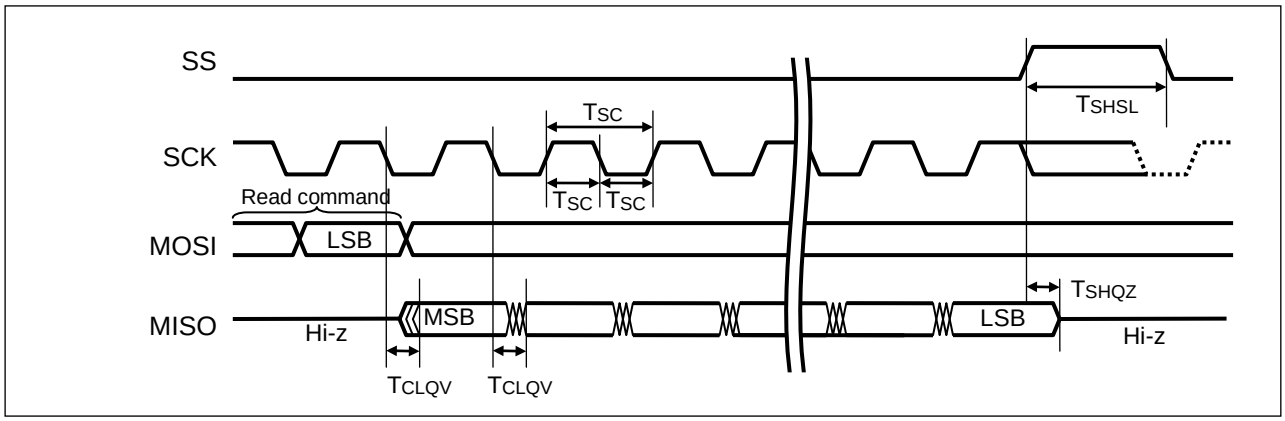


Figure 12-6 The latter part of serial I/F read cycle

Table 12-8 AC characteristics serial I/F access

Item	Symbol	Conditions	PCD4611A		PCD4621A		PCD4641A		Unit
			Min	Max	Min	Max	Min	Max	
Serial reference clock frequency	F_{SC}	C_L=40pF	-	15	-	15	-	15	MHz
Serial reference clock frequency	T_{SC}	C_L=40pF	67	-	67	-	67	-	ns
Serial clock High pulse width	T_{SCH}	-	20	-	20	-	20	-	ns
Serial clock Low pulse width	T_{SCL}	-	30	-	30	-	30	-	ns
SS active set up	T_{SLCH}	-	T_{SCL}	-	T_{SCL}	-	T_{SCL}	-	ns
SS deselection time	T_{SHSL}	-	T_{SC}	-	T_{SC}	-	T_{SC}	-	ns
SS active hold time	T_{CHSH}	-	T_{SCL}	-	T_{SCL}	-	T_{SCL}	-	ns
Data set up time	T_{DVCH}	-	5	-	5	-	5	-	ns
Data hold time	T_{CHDX}	-	5	-	5	-	5	-	ns
Output Disable time for SS↑	T_{SHQZ}	C_L=40pF	-	16	-	8	-	12	ns
Output delay time	T_{CLQV}	C_L=40pF	-	17	-	17	-	21	ns

13. External dimensions

13-1. PCD4611A external dimensions

Unit : mm

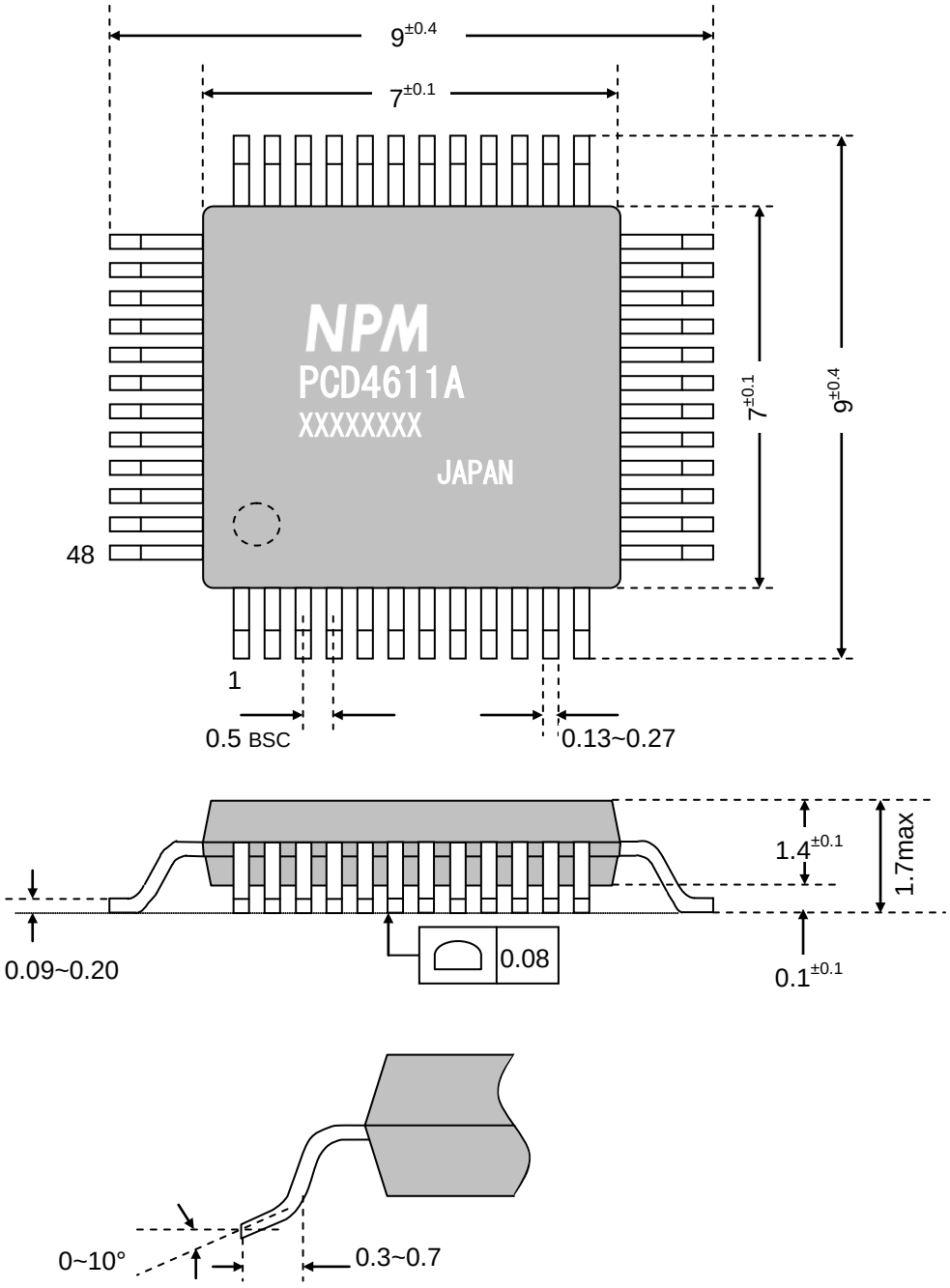


Figure 13-1 PCD4611A external dimensions (48-pin QFP)

13-2. PCD4621A external dimensions

Unit: mm

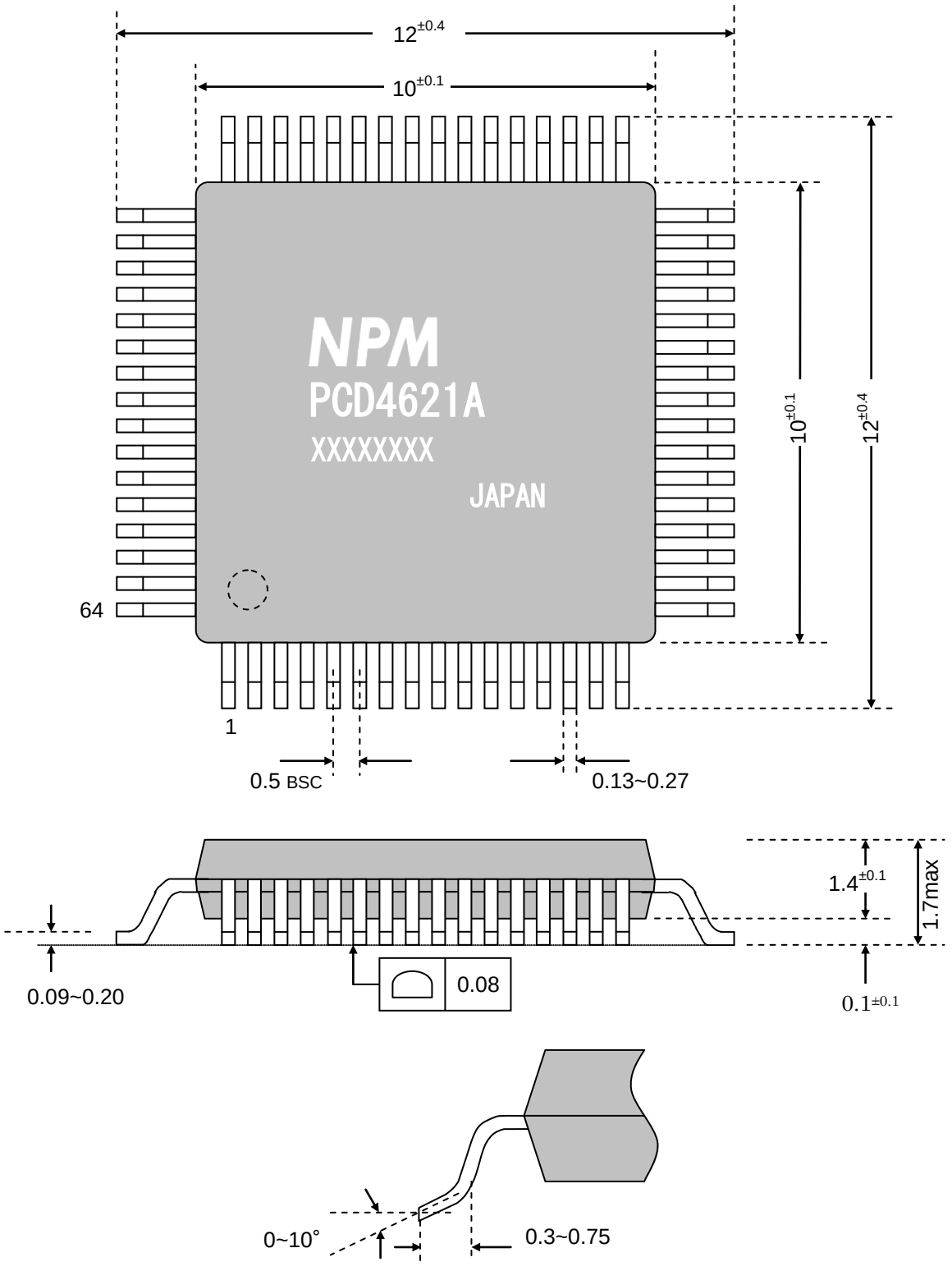


Figure 13-2 PCD4621A external dimensions (64-pin QFP)

13-3. PCD4641A external dimensions

Unit: mm

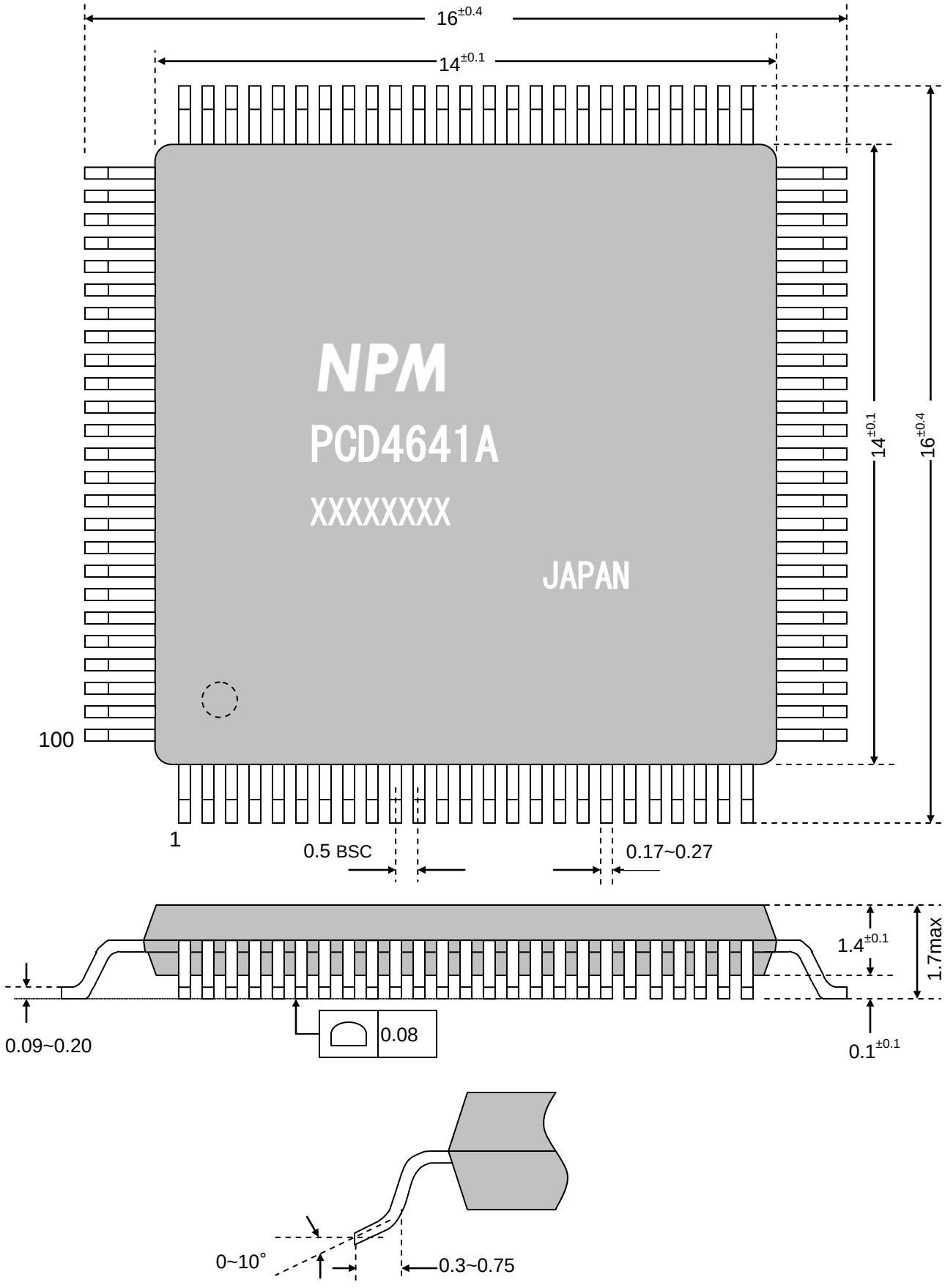


Figure 13-3 PCD4641A external dimensions (100-pin QFP)

14. Handling precautions

14-1. Hardware design precautions.

14-1-1. Basic precautions

1. Never exceed the absolute maximum ratings, even for a very short time.
2. Take precautions against the influence of heat in the environment, and keep the temperature around the LSI as cool as possible.
3. Please note that ignoring the following may result in latch-up phenomenon and may cause overheating and smoke.
   - Do not exceed the recommended conditions of the voltage on the Input terminals.
   - Consider the timing when turning ON/OFF the power.
   - Be careful not to introduce external noise into the LSI.
   - Hold the unused input terminals to +3.3 V or GND level.
   - Do not short-circuit the outputs.
   - Protect the LSI from inductive pulses caused by electrical sources that generate large voltage surges, and take appropriate precautions against static electricity.
4. Provide external circuit protection components so that overvoltage caused by noise, voltage surges, or static electricity is not fed to the LSI.
5. All signal terminals have TTL level interface and can be connected to 3.3 V-CMOS, TTL, and LVTTL devices. However, even if the output terminals are pulled up to 5 V, more than 3.3 V is not realized. Input terminals are not equipped with an over voltage prevention diode for the 3.3 V lines. If overvoltage may be applied due to a reflection, ringing, or inductive noise, we recommend inserting a diode to protect against over voltage.

14-1-2. PC board design

- In order to stabilize operation, we recommend using multi-layer board with 3.3V power source layer and GND layer separately.
- We recommend a capacitor that is approximately 0.1µF be placed between 3.3V and GND.

14-1-3. Handling of unused terminals

- Unused input terminal (with pull-up resistors) should be pulled up to 3.3V with 5k ~ 10k ohm or connected to 3.3V.
- Unused input terminal (without pull-up resistors) should be connected 3.3V or GND.
- Unused bidirectional terminals (with pull-up resistors) should be pulled up to 3.3V with 5k ~ 10k ohm
- Unused bidirectional terminals (without pull-up resistors) should be pulled up to 3.3V with 5k ~ 10k ohm or pulled down to GND.
- Make unused output terminal open (No connection).

14-1-4. About 5V tolerant

All signal terminals of this LSI have 5 V tolerant functions. However, please be careful about the following:

- Even though output terminals are pulled up to 5V, voltage does not become more than 3.3V. If more than 3.3V is needed as H level, level convert circuit should be connected externally.
- If more than 3.3V voltage is input to input (input / output) terminal with pull-up resistor, leakage occurs through internal pull-up resistors (40k~240k ohm) and input current increase.
- Input circuit has no diode for over overvoltage protection between terminal and 3.3V.

If there is any possiblity that voltage more than absolute maximum rating is input, add protection circuit externally.

14-1-5. About INT signal terminal

INT terminal is open drain terminal.

To use INT terminal, pull-up resistor (5k ohm ~ 10k ohm) should be connected externally.

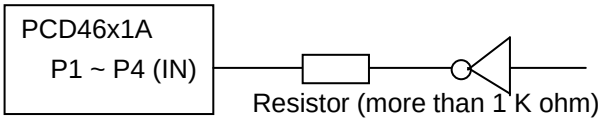
When using more than one LSI, INT terminals can be connected with one another in a wired-OR configuration.

14-1-6. When general-purpose input / output ports (P1 ~ P4) are used as general-purpose input

For compatibility with PCD45x1, at default setting, general-purpose input / output terminals are output terminals of sequence signals.

To use as input ports, insert series resistors for prevention against signal short circuit with external output circuit.

To use as output ports, series resistors are not needed. Please note that these are output level of sequence signal at default status.



More than 1 K ohm is needed to prevent the breakage of PCD46x1A. To prevent the breakage of an external circuit, select an appropriate resistor lest current exceeds the maximum output current of the external circuit.

14-1-7. Precautions in the case of use with parallel I/F

Serial I/F function was added in PCD46x1A. The RD and WR input terminals can be used to switch to the traditional parallel I/F. When the reset is cancelled, the serial interface will be activated if the both terminals are in low level. Other than that case, parallel interface will be activated.

In some CPU models, the initial conditions of the RD, WRoutput terminals are in floating (=general input ports). In that case, you will need external pull-up resistors in order to stabilize the initial conditions of the RD, WR terminals in high level.

In PCD46x1A, while the RST input is in low level, RD and WR signals will be sampled at the timing of rising edge of the CLK input. If the sampling results are both in low level, serial interface mode will be activated.

14-2. Software design precautions

1. If you use interrupt processing and access to PCD46x1 in interrupt processing, be careful about the following: If during accessing to PCD46x1 in normal program (non-interrupt program) an interrupt request occurs, interrupt program starts and PCD46x1 is accessed in interrupt program, the contents of register RD buffer (RegRBF) and register WR buffer (RegWBF) are changed.
   If LSI processing returns to normal in this situation, writing value to register may change a value or read a wrong value from register.
   Therefore, during accessing to PCD46x1 in normal program, make sure not to start up the interrupt program.
2. When you access to PCD46x1 from numeral tasks in multi-task processing, make sure not to switch tasks during accessing.

14-3. Mechanical precautions

14-3-1. When deceleration and stop is selected as stop by end limit detection signal

When a deceleration stop has been specified to occur when the EL input turns ON with RENV.ELDS=1, the motor starts deceleration when the EL input turns ON. Therefore, the motor stops after the

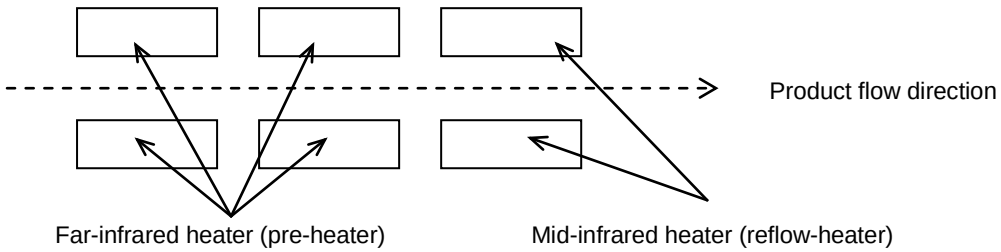
mechanical position passes over the EL position. In this case, be careful to avoid collisions of mechanical systems.

14-4. Precautions for transporting and storing LSIs

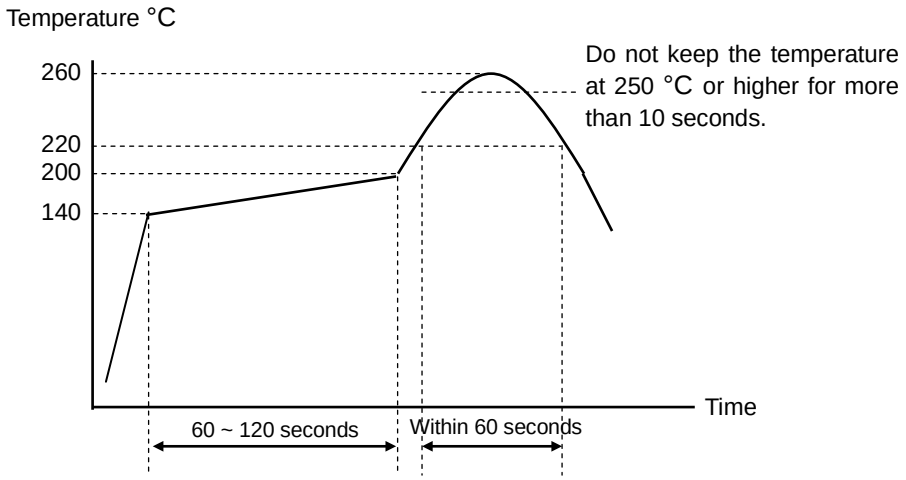
1. Always handle LSIs carefully. Throwing or dropping LSIs may damage them.
2. Do not store LSIs in a location exposed to water droplets or direct sunlight.
3. Do not store the LSI in a location where corrosive gases are present, or in excessively dusty environments.
4. Store the LSIs in an anti-static storage container, and make sure that no physical load is placed on the LSIs.

14-5. Precautions for mounting

1. In order to prevent damage caused by static electricity, pay attention to the following.
   - Make sure to ground all equipment, tools, and jigs that are present at the work site.
   - Ground the work desk surface using a conductive mat or similar apparatus (with an appropriate resistance factor). Do not allow work on a metal surface, which can cause a rapid change in the electrical charge on the LSI (if the charged LSI touches the surface directly) due to low resistance.
   - When picking up an LSI using a vacuum device, provide anti-static protection using a conductive rubber pick up tip. Anything which contacts the leads should have as high a resistance as possible.
   - When using a pincer that may make contact with the LSI terminals, use an anti-static model. Do not use a metal pincer, if possible.
   - Store unused LSIs in a PC board storage box that is protected against static electricity, and make sure there is adequate clearance between the LSIs. Never directly stack them on each other, as it may cause friction that can develop an electrical charge.
2. Operators must wear wrist straps which are grounded through approximately 1 M-ohm of resistance.
3. Use low voltage soldering devices and make sure the tips are grounded.
4. Do not store or use LSIs, or a container filled with LSIs, near high-voltage electrical fields, such those produced by a CRT.
5. To heat the entire package for soldering, dry the packages for 20 ~ 36 hours at 125 ± 5 °C. The packages should not be dried more than two times.
6. To reduce heat stress, we recommend far-infrared or mid-infrared reflow for soldering by infrared reflow. Make sure to observe the following conditions and do not reflow more than two times.



- Package and board surface temperatures must never exceed 260 °C and do not keep the temperature at 250 °C or higher for more than 10 seconds.



[Recommended temperature profile of a far/mid-infrared heater and hot air reflow]

7. When using hot air for solder reflows, the restrictions are the same as for infrared reflow equipment.
8. If you will use a soldering iron, the temperature at the leads must not exceed 350 degrees or higher and the time must not exceed for more than 5 seconds and more than twice per terminal.

14-6. Other precautions

1. When the LSI will be used in poor environments (high humidity, corrosive gases, or excessive amounts of dust), we recommend applying a moisture prevention coating.
2. The package resin is made of fire-retardant material; however, it can burn. When baked or burned, it may generate gases or fire. Do not use it near ignition sources or flammable objects.
3. This LSI is designed for use in commercial apparatus (office machines, communication equipment, measuring equipment, and household appliances). If you use it in any device that may require high quality and reliability, or where faults or malfunctions may directly affect human survival or injure humans, such as in nuclear power control devices, aviation devices or spacecraft, traffic signals, fire control, or various types of safety devices, we will not be liable for any problem that occurs, even if it was directly caused by the LSI. Customers must provide their own safety measures to ensure appropriate performance in all circumstances.

Appendix

Appendix A. Example of serial I/F access

- Write to a register

The followings are an example of “5-3-2-2 Write to a register.”

● Axis selection code = In the case of "0000 1001b"

Write data to each register of X axis and U axis with Device selection No. = “00b”

MOSI	Axis selection code	Command	X axis [7:0]	X axis [15:8]	X axis [23:16]	U axis [7:0]	U axis [15:8]	U axis [23:16]
MISO	Hiz							

● Axis selection code = In the case of "0000 0110b"

Write data to each register of Y axis and Z axis with Device selection No. = "00b"

MOSI	Axis selection code	Command	Y axis [7:0]	Y axis [15:8]	Y axis [23:16]	Z axis [7:0]	Z axis [15:8]	Z axis [23:16]
MISO	Hiz							

● Axis selection code = In the case of "0000 1110b"

Write data to each register of Y axis, Z axis and U axis with device selection No.= "00b"

MOSI	Axis selection code	Command	Y axis [7:0]	Y axis [15:8]	Y axis [23:16]	Z axis [7:0]	Z axis [15:8]	Z axis [23:16]	U axis [7:0]	U axis [15:8]	U axis [23:16]
MISO	Hiz										

● Axis selection code = In the case of "0000 1111b"

Write data to each register of X axis、Y axis、Z axis and U axis with device selection No. = "00b".

MOSI	Axis selection code	Command	X axis [7:0]	X axis [15:8]	X axis [23:16]	Y axis [7:0]	Y axis [15:8]	Y axis [23:16]	Z axis [7:0]	Z axis [15:8]	Z axis [23:16]	U axis [7:0]	U axis [15:8]	U axis [23:16]
MISO	Hiz													

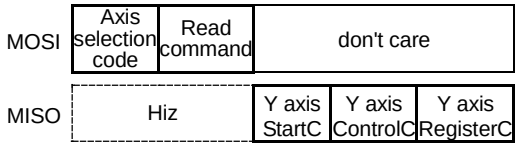
Note: If you write data that is more than the specified axis data, all written part beyond the specified is treated as write data of X axis.

- Read out a command

The following is an example of “5-3-3-1. Read command”

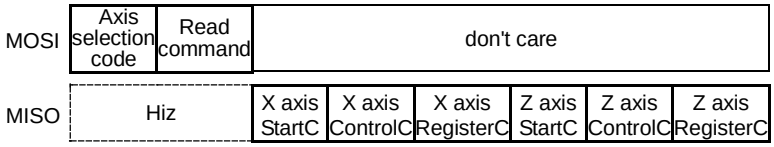
● Axis selection code = In the case of "0001 0010b"

Read out data from registers of X axis with device selection No. = "00b".



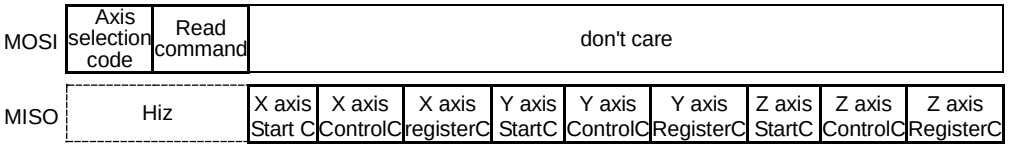
● Axis selection code = In the case of "0001 0101b"

Read out data from registers of X axis and Z axis with device selection No. = "00b".



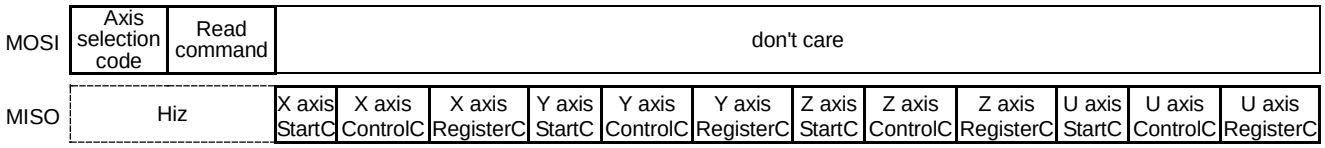
● Axis selection code =In the case of "0001 0111b"

Read out data from registers of X axis、Y axis、Z axis with device selection No. = "00b".



● Axis selection code = In the case of "0001 1111b"

Read out data from registers of X axis、Y axis、Z axis and U axis with device selection No. = "00b".



Note: If you try to read data that is more than the specified axis data, X axis data is output to read out beyond the specified.

- Read out status

The following is an example to “5-3-3-2. Read out status”.

● Axis selection code = In the case of "0001 0010b”

Read out stats of Y axis with device selection No. = "00b"

MOSI	Axis selection code	Read command	don't care		
MISO	Hiz		Y axis MSTS	Y axis RSTS_L	Y axis RSTS_H

● Axis selection code = In the case of "0001 0101b"

Read out status of X axis and Z axis with device selection No. = "00b"

MOSI	Axis selection code	Read command	don't care				
MISO	Hiz		X axis MSTS	X axis RSTS_L	X axis RSTS_H	Z axis MSTS	Z axis RSTS_L	Z axis RSTS_H

● Axis selection code =In the case of "0001 0111b"

Read out status of X axis、Y axis and Z axis with device selection No. = "00b"

MOSI	Axis selection code	Read command	don't care						
MISO	Hiz		X axis MSTS	X axis RSTS_L	X axis RSTS_H	Y axis MSTS	Y axis RSTS_L	Y axis RSTS_H	Z axis MSTS	Z axis RSTS_L	Z axis RSTS_H

● Axis selection code = In the case of "0001 1111b"

Read status of X axis、Y axis、Z axis and U axis with device selection No. = "00b".

MOSI	Axis selection code	Read command	don't care									
MISO	Hiz		X axis MSTS	X axis RSTS_L	X axis RSTS_H	Y axis MSTS	Y axis RSTS_L	Y axis RSTS_H	Z axis MSTS	Z axis RSTS_L	Z axis RSTS_H	U axis MSTS	U axis RSTS_L	U axis RSTS_H

Note: If you try to read data that is more than the specified axis data, X axis data is output to read out beyond the specified.

- Read out register

The following is an example of “5-3-3-3. Read out register”.

● Axis selection code = In the case of "0001 0010b"

Read data from register of Y axis with device selection No. = "00b"

MOSI	Axis selection code	Read command	don't care		
MISO	Hiz		Y axis [7:0]	Y axis [15:8]	Y axis [23:16]

● Axis selection code = In the case of "0001 0101b"

Read out data from register of X axis and Z axis with device selection No. = "00b".

MOSI	Axis selection code	Read command	don't care				
MISO	Hiz		X axis [7:0]	X axis [15:8]	X axis [23:16]	Z axis [7:0]	Z axis [15:8]	Z axis [23:16]

● Axis selection code = In the case of "0001 0111b"

Read out data from register of X axis、Y axis and Z axis with device selection No. = "00b"

MOSI	Axis selection code	Read command	don't care						
MISO	Hiz		X axis [7:0]	X axis [15:8]	X axis [23:16]	Y axis [7:0]	Y axis [15:8]	Y axis [23:16]	Z axis [7:0]	Z axis [15:8]	Z axis [23:16]

● Axis selection code = In the case of "0001 1111b"

Read out data from register of X axis、Y axis、Z axis and U axis with device selection No. = "00b"

MOSI	Axis selection code	Read command	don't care									
MISO	Hiz		X axis [7:0]	X axis [15:8]	X axis [23:16]	Y axis [7:0]	Y axis [15:8]	Y axis [23:16]	Z axis [7:0]	Z axis [15:8]	Z axis [23:16]	U axis [7:0]	U axis [15:8]	U axis [23:16]

Note: If you try to read data that is more than the specified axis data, X axis data is output to read out beyond the specified.

- Read out port status

The following is an example of “5-3-4. Read out general-purpose port status”.

● Axis selection code = In the case of "0010 1000b"

Read port status of U axis with device selection No. = "00b".

MOSI	Axis selection code	don't care	
MISO	Hiz	U axis PORT	

● Axis selection code = In the case of "0010 0110b"

Read out port status of Y axis and Z axis with device selection No. = "00b".

MOSI	Axis selection code	don't care	
MISO	Hiz	Y axis PORT	Z axis PORT

● Axis selection code = In the case of "0010 1101b"

Read port status of X axis, Z axis and U axis with selection No. = "00b"

MOSI	Axis selection code	don't care		
MISO	Hiz	X axis PORT	Z axis PORT	U axis PORT

● Axis selection code = In the case of "0010 1111b"

Read port status of X axis, Y axis, Z axis and U axis with device selection No. = "00b"

MOSI	Axis selection code	don't care			
MISO	Hiz	X axis PORT	Y axis PORT	Z axis PORT	U axis PORT

Note: If you try to read data that is more than the specified axis data, X axis data is output to read out beyond the specified.

- Read out main status

The following is an example of “5-3-5. Read out main status”.

● Axis selection code = In the case of "0011 1000b"

Read status of U axis with device selection No. = "00b".

MOSI	Axis selection code	don't care
MISO	Hiz	U axis MSTS

● Axis selection code = In the case of "0011 0110b"

Read status of Y axis and Z axis with device selection No. = "00b"

MOSI	Axis selection code	don't care	
MISO	Hiz	Y axis MSTS	Z axis MSTS

● Axis selection code = In the case of "0011 1101b"

Read status of X axis, Z axis and U axis with device selection No. = "00b".

MOSI	Axis selection code	don't care		
MISO	Hiz	X axis MSTS	Z axis MSTS	U axis MSTS

Note: If you try to read data that is more than the specified axis data, X axis data is output to read out beyond the specified.

● Axis selection code = In the case of "0011 1111b"

Read out status of X axis, Y axis, Z axis and U axis with device selection No. = "00b"

MOSI	Axis selection code	don't care			
MISO	Hiz	X axis MSTS	Y axis MSTS	Z axis MSTS	U axis MSTS

Note: If you try to read data that is more than the specified axis data, X axis data is output to read out beyond the specified.

Appendix B. Difference from PCD45x1

B1. Outline of Differences

1. PCD46x1A control software is downward compatible with PCD4511, PCD4521 and PCD4541.
   See “5-2. How to access with parallel I/F” in detail.
2. Because the power supply voltage, package and terminal assignment of PCD46x1 are different from those of PCD4511, PCD4521 and PCD4541, you need to prepare a new printed board.
3. 3.3 V single power supply (Signal terminals have 5 V tolerance functions.)
4. The package was downsized.
5. The Ambient operating temperature is -40 ~ +85 °C.
6. You can select output pulse mode from two-pulse mode ((+) pulse and (-) pulse)) and common pulse mode (pulse and direction signal).
7. The maximum output frequency is 2.4 [Mpps]. (When speed magnification is 300 times)
8. The function to set a ramping-down point automatically is added.
9. 24-bit current position counter is added for control of current position.
10. Wait control terminal (WRQ) is added for interface with CPU.
11. PH1 ~ PH4 terminals for sequence signal output are used as general-purpose input / output ports. If sequence signal output is not used, these can be used as general-purpose input terminals.
12. The function to monitor the status of U/Band F/H input terminals to set sequence signal output is added. If sequence signal output is not used, these can be used as general-purpose input terminals.
13. You can select the method of stop by ORG, +EL, -EL, STP signals. (To stop immediately or to decelerate and stop)
14. Serial I/F is added to interface with CPU
15. With serial I/F, D0 ~ D5 can be used as common ports (SP0 ~ SP5)

B2. Specification comparative table

Differences are shown with hatching in the following table.

Item	PCD46x1A standard	PCD45x1 standard
Power source	3.0 ~ 3.6[V]	4.5 ~ 5.5[V]
Reference clock	4.9152 [MHz] standard (Max. 10 [MHz])	Same as PCD46x1A
CPU I/F	Parallel I/F: 8 bit Serial I/F: Synchronous four wire serial	Parallel I/F: 8 bit
Positioning pulses setting range	0 ~ 16,777,215 pulses	Same as PCD46x1A
Speed setting step range	1 ~ 8,191 steps	Same as PCD46x1A
Recommended speed magnification range	1 ~ 300 times (reference clock: 4.9152[MHz]) When 1x 1 ~ 8,191 pps When 2x 2 ~ 16,382 pps When 300x 300 ~ 2,457,300 pps	1 ~ 50 times
Number of registers for setting the speed	Two (FL and FH speed)	Same as PCD46x1A
Ramping-down point setting range	0 ~ 16,777,215 (24 bit)	0~65,535 (16 bit)
Ramping-down point setting method	Manual or auto setting	Only manual setting
Acceleration / deceleration rate setting range	1 ~ 65,535 (16 bit)	2~1,023 (10 bit)
Current position counter	24 bit Up/down counter one circuit/ axis	None
Typical operations	− Continuous operation − Origin return operation − Positioning operation − Timer operation	Same as PCD46x1A
Typical functions	− Linear acceleration and deceleration / S-curve acceleration and deceleration − Immediate stop and decelerating stop − Speed change − External start and external stop function − Idling pulse output function − Excitation sequencing output for 2-phase stepper motor − 4 general-purpose input and output ports / axis (They also can be used as sequence output) − 6 common ports (available only with serial I/F)	Same as PCD46x1A except general-purpose port function and common ports
Ambient operating temperature	-40 ~ +85℃	0 ~ +85℃
Storage temperature	-65 ~ +150℃	-40 ~ +125℃
Package	PCD4611A: 48-pin QFP (Mold section: 7.0× 7.0 mm) PCD4621A: 64-pin QFP (Mold section: 10.0×10.0 mm) PCD4641A: 100-pin QFP (Mold section :14.0×14.0 mm)	PCD4511: 44-pin QFP (10.0×10.0 mm) PCD4521: 64-pin QFP (20.0×14.0 mm) PCD4541: 100-pin QFP (20.0×14.0 mm)
Chip design	C-MOS	Same as PCD46x1A

B3. Name change of internal registers.

The description of register name is changed from register No. to abbreviation of usage in manual.

Register name		function
PCD46x1A	PCD45x1	
RMV register	R0 register	Preset feed amount / confirm remaining pulses
RFL register	R1 register	Set FL speed
RFH register	R2 register	Set FH speed
RUD register	R3 register	Set acceleration / deceleration rate
RMG register	R4 register	Set magnification
RDP register	R5 register	Set ramping-down point
RIDL register	R6 register	Set idling pulse
RENV register	R7 register	Set environmental data
RCUN register	-	Current position counter
RSTS monitor	-	Extended status monitor
RIOP register	-	Set general-purpose port
RSPO register	-	Common port output setting / monitor
RSPM register	-	Common port setting

B4. Register

Bit length is extended and registers are added.

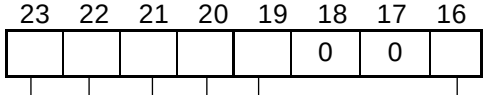
register	Description	PCD46x1A		PCD45x1	
		Bit width	Setting range	Bit width	Setting range
RUD	Set acceleration / deceleration rate	16	1 ~ 65,535	10	2 ~ 1,023
RDP	Set ramping-down point	24	0 ~ 16,777,215	16	0~65,535
RENV	Set environmental data	16	0000h ~ FFFFh	1	0~1 ∗1
RIDC	Product information code ∗4	8	00h ~ 40h	8	00h ~ C9h
RCUN	Current position counter	24	0 ~ 16,777,215 or -8,388,608 ~ +8,388,607	-	-
RIOP	Set general-purpose port	6	0 ~ 3Fh ∗2	-	-
RSPO	Common port output setting / monitor	6	0 ~ 3Fh ∗3	-	-
RSPM	Common port setting	6	0 ~ 3Fh ∗3	-	-

∗1: In PCD45x1 series, only PCD4541 has RENV register.

∗2: Cannot be accessed in PCD45x1 compatible mode and PCD4500 compatible mode

∗3: Available only with serial I/F.

∗4: Comparison between Product information code of PCD45x1 and PCD46x1A



Compatible mode monitor (＝ RENV.46MD)

Chip identification monitor

00010b: PCD4511　　10011b: PCD4611A

00100b: PCD4521　　10101b: PCD4621A

01000b: PCD4541　　11001b: PCD4641A

B5. Electrical Characteristics

Absolute maximum ratings

Item	Symbol	PCD46x1A	PCD45x1	Unit
Power supply voltage	V_{DD}	-0.3 ~ 4.0	-0.3 ~ +7.0	V
Input voltage	V_{IN}	-0.3 ~ +7.0	-0.3 ~V_{DD} + 0.3	V
Output current	I_{IN}	-	±10	mA
Storage temperature	T_{stg}	-65 ~ +150	-40 ~ +125	℃

Recommended operating conditions

Item		Symbol	PCD46x1A	PCD45x1	Unit
Power supply voltage		V_{DD}	+3.0 ~ +3.6	+4.5 ~ +5.5	V
Ambient temperature		T_a	-40 ~ +85	0 ~ +85	℃
Low level input voltage	1)	V_{IL}	-0.3 ~ +0.8	0 ~ +0.8	V
	2)		-0.3 ~ +0.8	0 ~ +1.0	
High level input voltage	1)	V_{IH}	+2.0 ~ +5.8	+2.2 ~ V_{DD}	V
	2)		+2.0 ~ +5.8	+4.0 ~ V_{DD}	

1) Other than CLK input
2) CLK input

DC characteristics

Item		Symbol	Condition	PCD46x1A	PCD45x1	Unit
Current consumption	1 axis	I_{DD}	1)	6	17 max	mA
	2 axis		1)	10	34 max	
	4 axis		1)	20	65 max	
Output leakage current		I_{OZ}	-	-1 ~ +1	-10 ~ +10	µA
Input capacitance		C_{IN}	-	10 max	7 max	pF
L level input current	2)	I_{IL}	V_{IN} = GND	-1	-10	µA
	3)			-90	-200	
H level input current	4)	I_{IH}	V_{IN} = V_{DD}	+1	+10	µA
L level output current	5)	I_{OL}	-	6 max	8 max	mA
	6)			6 max	16 max	
	7)			6 max	16 max	
H level output current	5)	I_{OH}	-	-6 max	-8 max	mA
	6)			-6 max	-16 max	
L level output voltage		V_{OL}	I_{OL} = max	0.4 max	0.4 max	V
H level output voltage		V_{OH}	I_{OH} = -1µA	V_{DD} - 0.4 min	V_{DD} - 0.05 min	V
			I_{OH} = max	V_{DD} - 0.4 min	2.4 min	
Internal pull-up register		R_{PU}	-	40 ~ 240	25 ~ 500	K ohm

1) Reference clock 10 [MHz], 4,999,390 [pps] output, No load.
2) D0/SP0 ~ D7 / MOSI, A0 / DS0 ~ A3, RD, WR, CS / SS, CLK
3) ORG, +EL, -EL, -SD, +SD, STA, STP, U/B, F/H, RST
4) Terminal 2 or 3
5) D0/SP0 ~ D7 / MOSI and OTS, BSY, +PO / PLS, -PO / DIR, PH1 / P1 ~ PH4 / P4 of PCD4x21 and PCD4x41
6) OTS, BSY, +PO / PLS, -PO / DIR, PH1 / P1 ~ PH4 / P4 of PCD4x11 (1 axis)
7) INT

Appendix C. Internal monitor (with parallel I/F)

PCD46x1 mode

RCM3 ~ 0	Address			
	A1 = 1, A0 = 1	A1 = 1, A0 = 0	A1 = 0, A0 = 1	A1 = 0, A0 = 0
0000b	RMV upper data	RMV middle data	RMV lower data	Main status
0001b	Start mode command	RFL upper data	RFL lower data	Main status
0010b	Control mode command	RFH upper data	RFH lower data	Main status
0011b	Register selection command	RUD upper data	RUD lower data	Main status
0100b	Output mode command	RMG upper data	RMG lower data	Main status
0101b	RDP upper data	RDP middle data	RDP lower data	Main status
0110b	RSPD upper data	RSPD lower data	RIDL data	Main status
0111b	RIDC data	RENV upper data	RENV lower data	Main status
1000b	RCUN upper data	RCUN middle data	RCUN lower data	Main status
1001b	(Always 00h)	RSTS upper data	RSTS lower data	Main status
1010b	(Always 00h)	(Always 00h)	RIOP data	Main status
1011b	(Always 00h)	(Always 00h)	(Always 00h) *1	Main status
1100b	(Always 00h)	(Always 00h)	(Always 00h) *1	Main status
1101b ~ 1111b	(Always 00h)	(Always 00h)	(Always 00h)	Main status

*1: Description is like shown in the table because of parallel I/F.

PCD45x1 compatible mode

RCM2 ~ 0	Address			
	A1 = 1, A0 = 1	A1 = 1, A0 = 0	A1 = 0, A0 = 1	A1 = 0 ,A0 = 0
000b	RMV upper data	RMV middle data	RMV lower data	Main status
001b	Start mode command	RFL upper data	RFL lower data	Main status
010b	Control mode command	RFH upper data	RFH lower data	Main status
011b	Register selection command	RUD upper data	RUD lower data	Main status
100b	Output mode command	RMG upper data	RMG lower data	Main status
101b	RENV lower data	RDP upper data	RDP lower data	Main status
110b	RSPD upper data	RSPD lower data	RIDL data	Main status
111b	RIDC data	RSTS upper data	RSTS lower data	Main status

PCD4500 compatible mode

RCM2 ~ 0	Address			
	A1 = 1, A0 = 1	A1 = 1, A0 = 0	A1 = 0, A0 = 1	A1 = 0, A0 = 0
000b	RMV upper data	RMV middle data	RMV lower data	Main status
001b ~ 111b	(Always 00h)	(Always 00h)	(Always 00h)	Main status

MEMO