	Notification of revision of PCD2112	Control No: DBZ0175-0
		Date: April 04, 2018
		Nippon Pulse Motor Co., Ltd. Motion Control Division ASIC Department

Dear customers:

Thank you for your business with Nippon Pulse Motor.
We are sending this letter to inform you the revision work of PCD2112 LSI. The revision this time is in accordance with the termination of PCD2112 production in the ASIC vender that we have asked the production.
Right now, we are in the revision process to transfer the production of PCD2112 to a different LSI manufacturer. The difference between the revised version and existing version is described as follows.
If you have any questions, please feel free to contact us.
Thank you for your kind attention.

Sincerely yours,
Nippon Pulse Motor Co., Ltd.

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1. Revisions

Basically, development of revised version is being proceeded so as not to cause functional differences. We made some corrections, which should have little influence on software created by customers. In the following sections, we explains those corrections.
In the following explanations, the existing product is referred to as "PCD2112", and the revised product is as "PCD2112***A***".

1-1. Terminals

The existing PCD2112 has some output buffers whose output capacities are 9 mA. However, the revised version, 2112A, has no 9 mA output buffers, so 12 mA type output buffers will used, instead. In this case it will be for high speed. There are six high-speed terminals, and the possible high-speed terminal is only for pulse train output (OUT). The other five terminals are for low operating speed.

The comparisons between 2112 and 2112A terminals are shown in a table from the next page:

				PCD2112			PCD2112A		
No.	Terminal name	I/O	Description	Current	5V Withstand voltage	Other	Current	5V Withstand voltage	Other
1	PO	B	General-purpose I/O terminal 0	6mA	✓		6mA	✓	
2	P1	B	General-purpose I/O terminal 1	6mA	✓		6mA	✓	
3	#RST	I	Reset	–	✓		–	✓	
4	#INT	O	Interrupt request	6mA	✓	three state	6mA	✓	three state
5	MODE	I	Operation mode	–	✓		–	✓	
6	GND	I	GND						
7	CLK	I	Reference clock	–	✓		–	✓	
8	VDD	I	+ 3.3V						
9	PA/PDR	I	Pulser A / (+) direction operation	–	✓		–	✓	
10	PB/MDR	I	Pulser B / (-) direction operation	–	✓		–	✓	
11	EA	I	Encoder A phase	–	✓		–	✓	
12	EB	I	Encoder B phase	–	✓		–	✓	
13	EZ	I	Encoder Z phase	–	✓		–	✓	
14	ORG	I	Origin position sensor	–	✓		–	✓	
15	SD	I	Slow-down sensor (common in both ± directions)	–	✓		–	✓	
16	MEL	I	(-) end limit	–	✓		–	✓	
17	PEL	I	(+) end limit	–	✓		–	✓	
18	GND	I	GND						
19	ERC/CDW	O	Clear deviation counter/current reduction	9mA	✓		12mA	✓	Hi Speed
20	#BSY/#END	O	Busy/Operation complete	9mA	✓		12mA	✓	Hi Speed
21	MELL	I	MEL input logic	–	✓		–	✓	
22	PELL	I	PEL input logic	–	✓		–	✓	
23	INP/FH	I	In position / Full (L), half (H)	–	✓		–	✓	
24	UB	I	Unipolar (L) / Bipolar	–	✓		–	✓	
25	GND	I	GND						
26	OUT/PH1	O	Driving pulse /1-phase excitation signal	9mA	✓		12mA	✓	Hi Speed
27	DIR/PH2	O	Driving pulse/ 2-phase excitation signal	9mA	✓		12mA	✓	Hi Speed
28	P2/PH3	O	General-purpose output terminal 2 /3-phase excitation signal	9mA	✓		12mA	✓	Hi Speed
29	P3/PH4	O	General purpose output terminal 3 /4-phase excitation signal	9mA	✓		12mA	✓	Hi Speed
30	VDD	I	+3.3 V						
31	GND	I	Input terminal for shipment inspection (GND)	–			–		
32	GND	I	Input terminal for shipment inspection (GND)	–			–		
33	MTYP	I	Pulse train output or Sequence	–	✓		–	✓	
34	#CSO	O	CS output for EEPROM	6mA	✓		6mA	✓	
35	DI	B	For serial communication: Data input	6mA	✓		6mA	✓	

36	DO	B	For serial communication: Data output	6mA	✓		6mA	✓	
37	GND	I	GND						
38	#CS	B	Serial communication: CS input	6mA	✓		6mA	✓	
39	GND	I	GND						
40	SCK	B	Serial communication: Synchronous clock	6mA	✓		6mA	✓	
41	VDD	I	+ 3.3V						
42	#STA	B	External start	6mA	✓		6mA	✓	
43	STP	I	External stop	–	✓		–	✓	
44	A0/PS0	I	Device selection 0	–	✓		–	✓	
45	A1/PS1	I	Device selection 1	–	✓		–	✓	
46	PS2	I	Pattern selection 2	–	✓		–	✓	
47	PS3	I	Pattern selection 3	–	✓		–	✓	
48	PS4	I	Pattern selection 4	–	✓		–	✓	

1-2. If FH speed is changed during positioning operation; it will not slow down properly.

In positioning operations with S-curve acceleration/deceleration, if speed is changed before reaching the target position, the slow down point (position) cannot be appropriate (it does not occur in linear acceleration/deceleration operations); We will revise it so that it will slow down properly.

Regarding this issue, see a notice on page 50 in section “9.5. Changing the speed pattern during operation” in PCD2112 User’s Manual (the 4th revision).

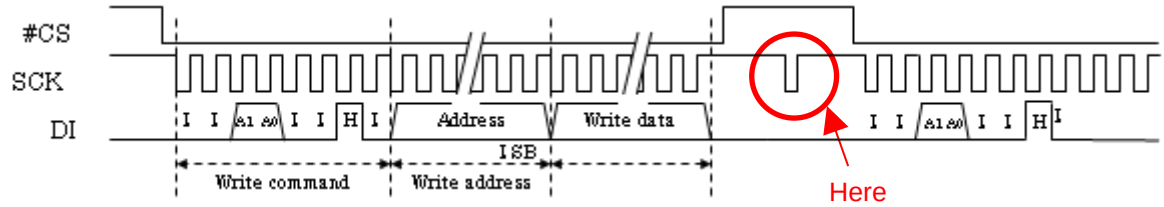
1-3. When an emergency stop command is issued while stopped, the following start command will be disabled. If an emergency stop command is written while stopped, it is stored and an error occurs at the following start command execution. At this point, we recommend our users a software countermeasure "to write a dummy stop command after writing the emergency stop command".

We revised the LSI so that this error will never occur at the following start command. If a dummy stop command is used in the software you have created with existing 2112, the same operation before the revision will be performed with 2112A.

1-4. Extra specifications for control when changing SPI address

As for the "Note" on page 22 in section "5-9. How to identify a PCD when multiple PCDs are connected” in the PCD2112 User's Manual, it can be an extra specification in software creation.

Note: To switch between PCD2112s, you have to supply SCK for at least one clock cycle, while #CS = H level.
The CPU must change the output logic of the SCK signal temporarily.



When switching addresses, it was conditional to input clock signals through SCK input terminal while maintaining # CS = High. However, this condition is eliminated and the address can be switched regardless of input or no-input of clock signals.

Even if a clock signal is input through SCK input terminal while maintaining # CS = High with the software created, 2112A performs the same before this revision.

1-5. Change of specific circuits of the previous ASIC vendor

Input and output buffers and clock trees, etc. with the previous vendor are all changed to the parts made by vendors after revision.

Although this change can maintain functional compatibility, differences in performance will occur. These differences cannot be avoided when changing ASIC vendors.

For details, refer to "1-1. Terminals" and “2. Performance differences in accordance with this ASIC vendor change" in this notification. .

1-6. “Reading ID number” function is added in 2112A. .

A function to distinguish between 2112 and 2112A by software is added. .

The first 4 bytes of the current memory map is available as a reserved area. We will use 2 bytes out of the area to accommodate ID numbers to be read.

If you do not issue a newly added "read-only command” before reading ID number, the result of reading the first 4 bytes has the same result as 2112.

With the software created for 2112 in the past, the operation with 2112A will be the same because “read-only command” has not been used in the past..

2. Performance differences in accordance with this ASIC vendor change.

2-1. Absolute maximum ratings

(Vss=0V)

			PCD2112	PCD2112A	Unit
Item	Symbol	Condition	Rating	Rating	
Supply voltage	V_{DD}		−0.5～+4.6	−0.3～+4.0	V
Input voltage	V_{IN}	$V_{IN}<V_{DD}$+0.5V	−0.5～+4.6	−0.3～+3.8	V
Input voltage (5V･I/F)	V_{IN}	$V_{IN}<V_{DD}$+3.0V	−0.5～+6.6	−0.3～+7.0	V
Output voltage(5V･I/F)	V_O	$V_{IN}<V_{DD}$+3.0V	−0.5～+6.6	−0.3～+7.0	V
Input current (=6mA)	I_O		20	±30	mA
Output current (>6mA)	I_O		30 (9mA)	±30 (12mA)	mA
Storage temperature	T_{STC}		−65 to+150	−65 to+150	℃

2-2. Recommended operating conditions

(Vss=0V)

		PCD2112	PCD2112A	Unit
Supply voltage	V_{DD}	+3.3±0.3	+3.3±0.3	V
Input voltage	V_{IN}	V_{DD}	−0.3 to+3.6	V
Input voltage (5V･I/F)	V_{IN}	to 5.5	to 5.8	V
Ambient temperature	T_a	−40 to+85	−40 to+85	℃

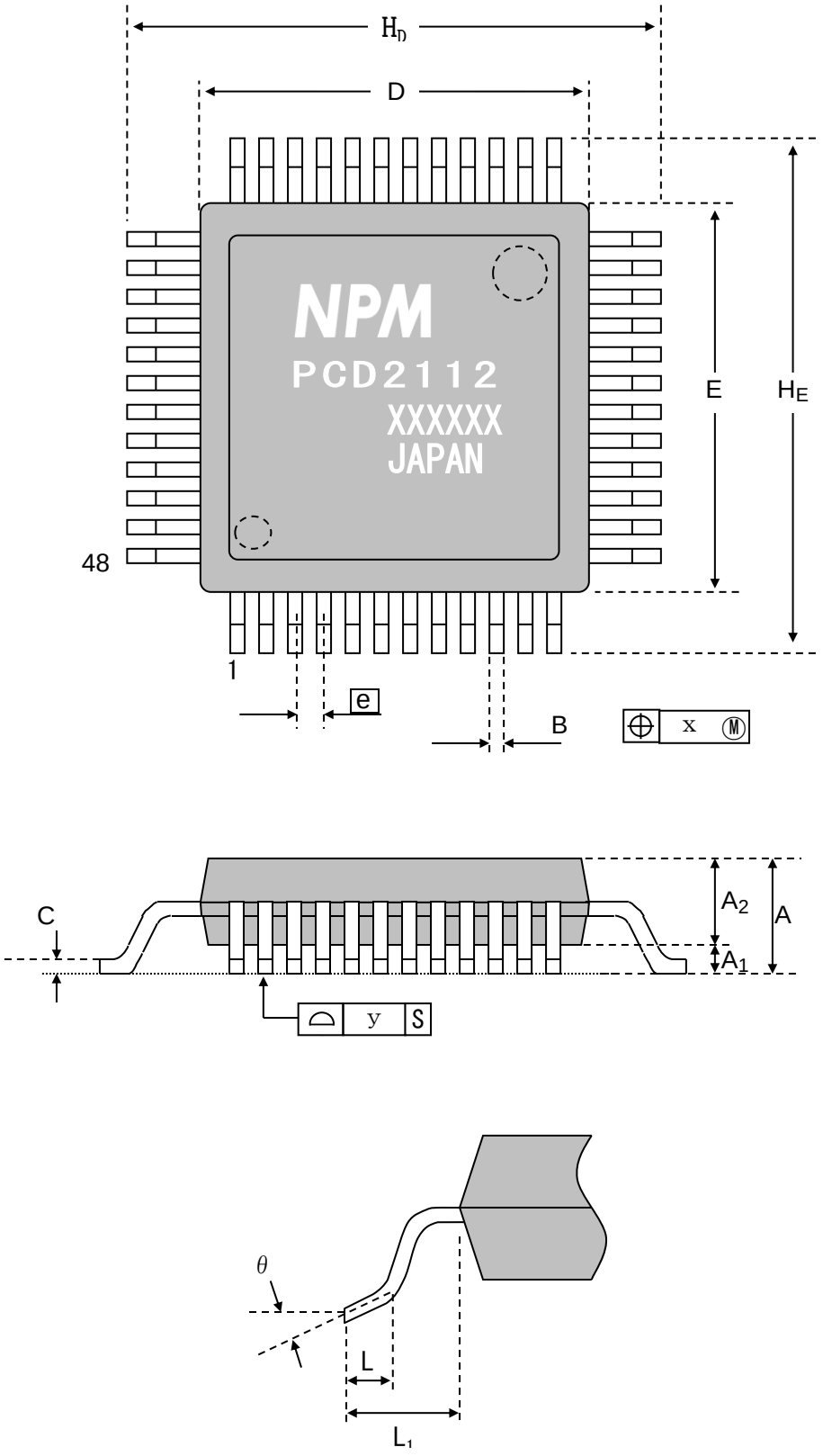
2-3. DC characteristics

(Vss=0V)

Item	Symbol	Condition	PCD2112		PCD2112A		Unit
			Min	Max	Min	Max	
Current consumption	I_{dd}	CLK=9.8304MHz, No load		16		N/A	mA
		CLK=20.000MHz, No load		31		N/A	mA
Input capacitance				9		10	pF
L level input current	I_{IL}	V_I = GND		±1.0		±1	μA
H level input current	I_{IH}	$V_I = V_{DD}$	28	190		30	μA
L level input voltage	V_{IL}		0	0.8	-0.3	0.8	V
H level input voltage	V_{IH}	$V_{IL} < V_{DD}+3.0V$	2.0	5.5	2.0	5.8	V
L level output voltage	V_{OL}	I_{OL}=0mA		0.1		V_{SS}+0.4	V
H level output voltage	V_{OH}	I_{OH}=0mA	V_{DD}-0.2		V_{DD}-0.4		V
L level output voltage	I_{OL}	6mA output (V_{OL}=0.4V)		6.00		6	mA
		≧9mA output(V_{OL}=0.4V)		9.00		12	
H level output voltage Input fall time	I_{OH}	6mA output(V_{OH}=2.4V)	-3.00		-6		mA
		≧9mA output(V_{OH}=2.4V)			-12		
Input rise time	Tr		0	200	0	50	ns
Internal pull down resistance	Tf		0	200	0	50	ns
Current consumption	R_{PD}	$V_I = V_{DD}$	18.9	107.1	40	240	kΩ

2-4. Package dimensions

The basic dimensions are the same; there is no big difference.



Symbol		PCD2112	PCD2112A
D	Min	6.8	6.90
	Typ	7.0	7.00
	Max	7.2	7.10
E	Min	6.8	6.90
	Typ	7.0	7.00
	Max	7.2	7.10
A	Min	1.0	-
	Typ	1.1	-
	Max	1.2	1.20
A_1	Min	0.05	0.00
	Typ	0.10	0.10
	Max	0.15	0.20
A_2	Min	-	0.90
	Typ	1.0	1.00
	Max	-	1.10
e	Min	-	-
	Typ	0.5	0.50
	Max	-	-
B	Min	0.18	0.17
	Typ	0.22	0.22
	Max	0.27	0.27
C	Min	0.10	0.09
	Typ	0.17	0.15
	Max	0.20	0.20
θ	Min	0°	0°
	Typ	3°	5°
	Max	7°	10°
L	Min	0.45	0.30
	Typ	0.6	0.50
	Max	0.75	0.70
L_1	Min	0.8	0.80
	Typ	1.0	1.00
	Max	1.2	1.20
H_D	Min	8.8	8.60
	Typ	9.0	9.00
	Max	9.2	9.40
H_E	Min	8.8	8.60
	Typ	9.0	9.00
	Max	9.2	9.40
x	Min	-	-
	Typ	-	-
	Max	0.10	0.08
y	Min	-	-
	Typ	-	-
	Max	0.08	0.10

2-5. Precautions for installation

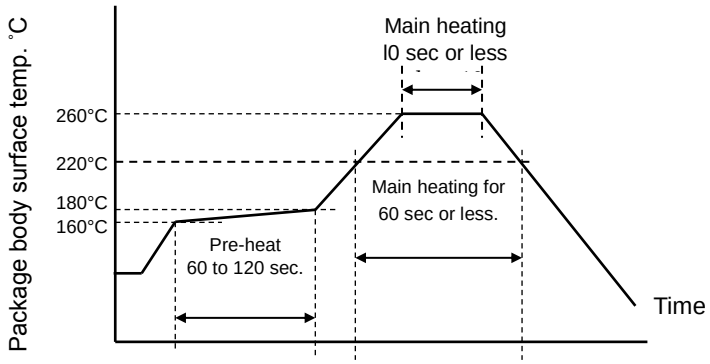
The shaded parts with parenthesis below are the revised points in PCD2112A:

1) Plastic packages absorb moisture easily, and they will become damp over time, even when stored in a room.
When damp LSIs are put in a reflow furnace, cracks may occur in the resin and the adhesive between the resin and frame may deteriorate.
The storage period before unpacking the chips from the moisture prevention bag is one year.

2) If moisture is probable, dry the packages thoroughly before any reflow operation.
Dry the packages 10(20) to 72(36) hours at 125˚C (125±5°C).
You can dry them up to one (two) time(s).
Basically, if an LSI is left for 7 days (30 days) after being unpacked from its moisture prevention bag, it must be dried.

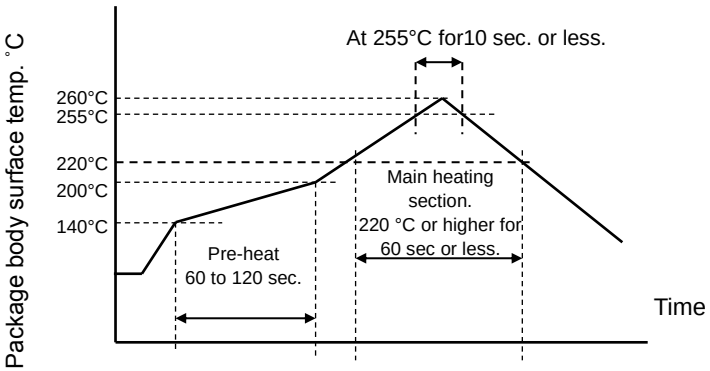
3) If the LSI will be soldered by heating the whole LSI package, such as with an infrared reflow system, conduct to solder within the range specified below, and limit the number of reflow events to three (two) times.
- Temperature profile: The temperature profile of the IR reflow furnace must be within the range shown in the figure below.
- We recommend that the chlorine content (mass rate %) of the rosin family flux should be 0.2% or less. (No description)

PDC2112



[Profile (for lead-free solder)]

PDC2112A



[Profile (for lead free solder)]

4) Soldering using the solder dipping method may cause rapid temperature changes in the package and may cause damage to the device. Do not use this method with these LSIs.

5) Hand soldering work using a soldering iron, please do the following conditions.
Tip maximum temperature 300 °C (350 °C), maximum 3 seconds (5 seconds) (per side of LSI).
Make sure that the soldering iron does not come into contact with parts other than lead parts such as package body.

- End of documents -